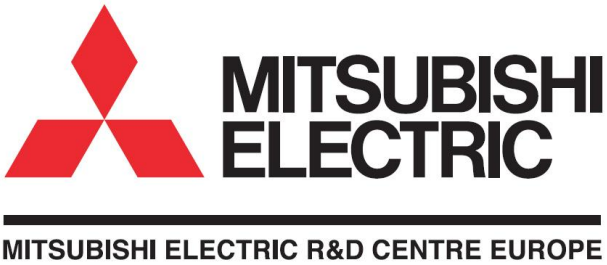

IEEE International Workshop On Integrated Power Packaging (IWIPP), Delft, Netherlands, April 2017

DOI: 10.1109/IWIPP.2017.7936757

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***Abstract*—The Printed-Circuit-Board (PCB) technology is attractive for power electronic systems as it offers a low manufacturing cost for mass production. In this paper, we present a procedure to design power inductors based on PCB. These inductors either use PCB for the winding only (Planar structure), or to host both the magnetic core and the winding (Toroidal PCB structure). The design procedure compares, in the form of a Pareto fronts, the two inductor structures over a large range of parameters (geometric parameters, magnetic materials), to identify the best candidates in terms of power losses and box volume. In this procedure, the core losses are taken into account using improved Generalized Steinmetz Equation (iGSE). The skin and proximity effects are considered using the AC resistance calculated with a FEM software. The inductor feasibility is checked from a mechanical perspective using the PCB design rules and from a thermal point of view with FEM simulation. A design case is presented for a 3.3 kW multi-cellular (3 interleaved cells) Power Factor Corrector (PFC). It is found that the planar design offers the most compact solution, but might present challenges regarding thermal management. The Toroidal PCB structure tends to be larger, but easier to cool.**

I. Introduction

Although it is a recent technology, embedding of power electronic components in Printed Circuit Board (PCB) has attracted interest from the industry, with products already available on the market [1]. This technology enables more integrated converters, with a single, consistent manufacturing process. PCBs present a low manufacturing cost for mass production. The passive components represent a large share (20 %) of a converter volume, on par with its cooling system and empty spaces [2]. Their integration in the PCB is therefore especially attractive. However, most studies focused on the integration of power semiconductor devices only, or on the integration of passive devices, but for very low power only (for converters with a power under a few tens of watts). Die embedding technology is commercially available from several PCB manufacturers (AT&S, ASE, Würth Electronik… [3]). Low-power or low-value capacitive devices are formed using capacitive layers [4] integrated in the PCB stack-up. Regarding magnetic devices, the investigations were mainly focused on low-power application using either no magnetic material at all ("coreless") [5], or cores with a small size. For example, in [6], two coupled inductors (3 μH each) for a load power of 30 W are embedded in a PCB of 4.5x4x0.25 = 4.5 cm^3. Transformer also can be embedded in PCB, like in [7] in which a 1.5x2.2x0.36 = 1.18 cm^3 - 2 W power supply is prototyped.

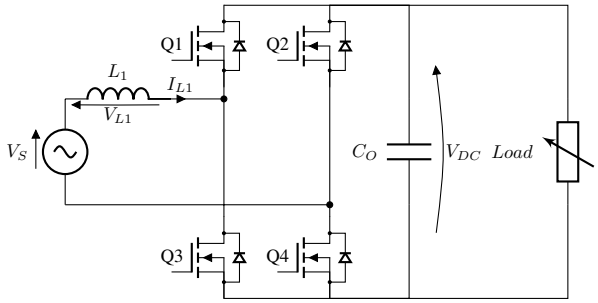


Figure 1: Single cell of a power factor corrector schematic

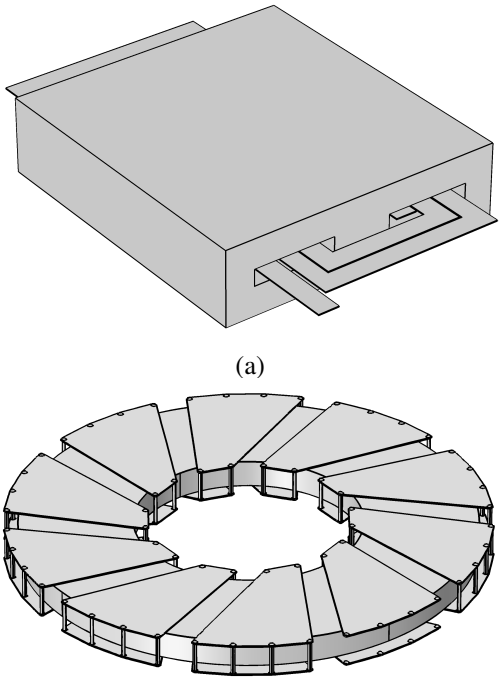
The design procedure presented in this paper is applied to the inductor of an interleaved Power Factor Corrector (PFC). The specifications of this converter are presented in the table I. The schematic of a single PFC cell is presented in the figure 1. There is no coupling between the inductors of each PFC cell. Note that the design procedure described here is part of a larger procedure (not described in this paper, for the sake of brevity), which aims at designing the smallest possible PFC, by evaluating the optimal number of interleaved cells, the optimal switching frequency and the amplitude of the input current ripple.

Two "integrated" inductor structures are investigated here (Fig. 2). The first structure is called "Planar", and is well established in the industry. It uses PCB copper traces for the winding and an external magnetic core clipped around. The second design is called "Toroidal PCB". The winding is also made by PCB copper traces and vias, but in this structure, the magnetic core in embedded in a cavity inside the PCB. Due to PCB manufacturing limitations, the core thickness is limited to 3 mm for a final thickness of the PCB of 3.2 mm. The main advantage of such integration approach is to make use of the free space inside the PCB. The PCB top side can then be used to mount SMD components, while the bottom side can be used for cooling. Both structures are investigated over a large range of geometrical parameters and magnetic materials, to identify the best candidates in terms of power losses and box volume.

In this paper, we firstly introduce the design procedure with its specifications and the magnetic design calculations. In particular, we detail the calculation of copper and core losses as well as a thermal model, which is then used to calculate

Input voltage range	85-260 V_{rms}
Output voltage range	280-370 V
Maximum input current	15 A_{rms}
Maximum output current	12 A
Maximum output power	3.3 kW
Volume (all inclusive)	0.6 L
Ambient temperature	-40 °C to +60 °C

Table I: PFC specifications



(a)

(b)

Figure 2: Geometry of the designs compared with magnetic core and winding (PCB traces and vias). The PCB core is not represented (a) Planar (b) Toroidal PCB

maximum temperature reached by the inductor. Using this procedure, we then present a comparison of both structures for different magnetic materials in the form of a Pareto fronts.

II. Design Procedure:

Inputs:

The flowchart in Fig. 3 describes the design procedure, which we implemented using MATLAB. Three sets of inputs are used. The first set is generated by the global converter design procedure and consists in the inductor value (L), and a vector which describes the inductor current waveform ($I_L(t)$). This waveform contains a low frequency component (50 Hz) and a high frequency component (switching frequency) (Fig. 4).

The second set of inputs is the magnetic material database which contains ferrite (single airgap) and powder (distributed airgap) materials. Each material is described using 5 parameters. The first parameter is the relative permeability (μ_r). The second one is the maximum induction (B_{sat}). The last three properties are the Steinmetz coefficients (k, α, β) used to calculate the core losses [8].

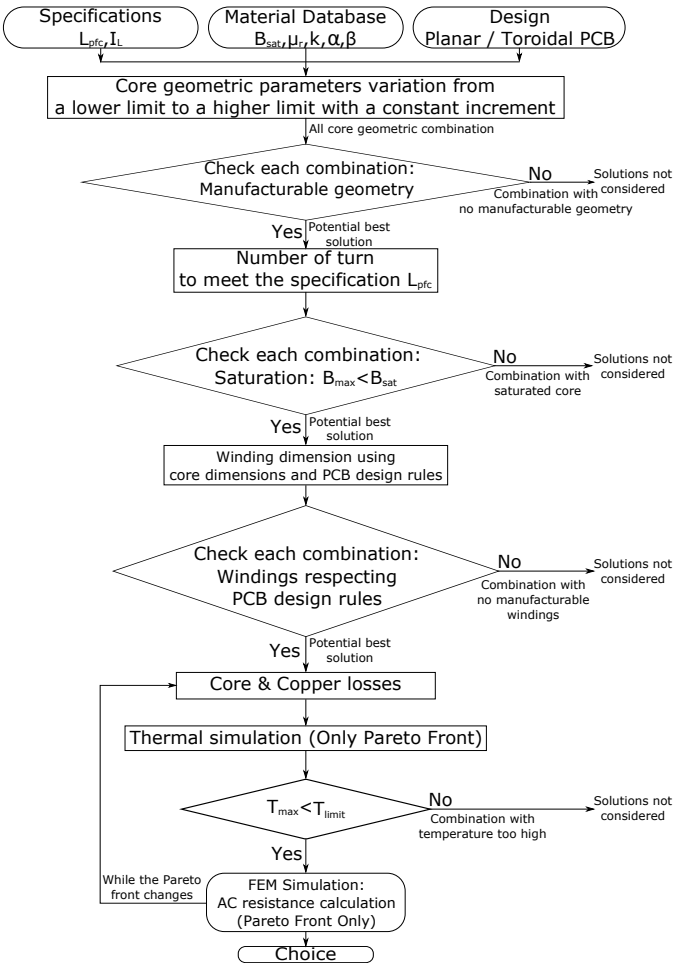


Figure 3: Flowchart of the design procedure

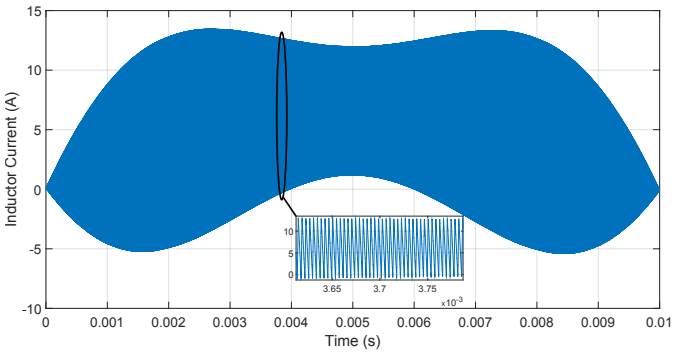


Figure 4: Inductor current waveform for a 3 cells interleaved PFC for the positive half period

The third set of inputs is the selected inductor structure: "Planar" or "Toroidal PCB", with its associated design rules listed in table II.

Magnetic Design:

The geometric parameters (i.e. for "Toroidal PCB": outer diameter, inner diameter and thickness) vary between a lower limit and a higher limit with constant increments. A design

Copper thickness	105 μm
PrePreg thickness	200 μm
Clearance	200 μm
Via drill tool diameter	350 μm
Via final diameter	250 μm

Table II: PCB design rules used for inductor design

matrix, containing all combinations of magnetic core geometric parameters is then generated. The combinations giving impossible geometries (e.g. inner diameter larger than outer diameter) are discarded. For each combination, i.e for each given core geometry, the magnetic path length (l_e) and the magnetic section (A_e) are calculated. They are used with the permeability of the chosen material to calculate the number of turns necessary to achieve the specified inductance value, using eq. (1).

$$L = \mu_0 \mu_r N^2 \frac{A_e}{l_e} \tag{1}$$

Some combinations lead to saturation of the magnetic core due to an excessive number of turns ($\mu_0 \mu_r N_{max} I_{max}/l_e > B_{Sat}$). These solutions are discarded. With the core geometry and the number of turns for each combination, the winding dimensions are calculated. In some cases, it is not possible to calculate dimensions which meet the design rules (in particular the clearance between copper tracks). These solutions are discarded.

Loss Calculation:

The inductor losses can be separated into core losses and copper losses.

As the inductor current has a complex waveform (a 50 Hz sinewave with a superimposed high frequency ripple), the calculation of the core losses is based on the improved Generalized Steinmetz Equation (iGSE, eq (2), [8]).

$$P_{v_i} = \frac{1}{T} \int_0^T k_1 |\frac{dB}{dt}|^{\alpha} (\Delta B])^{\beta - \alpha} dt \tag{2}$$

where:

$$k_1 = \frac{k}{(2\pi)^{\alpha-1} \int_0^{2\pi} |\cos\theta|^{\alpha} 2^{\beta-\alpha} d\theta} \tag{3}$$

where (k, α, β) are the Steinmetz coefficients, B is the flux waveform, T is the period of the signal and i is the index of the hysteresis loop. Indeed, the iGSE has to be applied on major and minor loops. The inductor current waveform presented in Fig. 4 generates one major loop per cycle, and many minor loops, which must be identified. Therefore, the flux density waveform is separated into two parts: rising & falling. The script begins parsing the rising part of the waveform (from the global minimum to the global maximum). The data is attributed to the major loop until the first local maximum is reached. The data is then associated with the first minor loop until the data goes through a local minimum and comes back to the first local maximum. From this point to the second local maximum, the data is added to the major loop. At the second local maximum, the second minor loop begins. This procedure

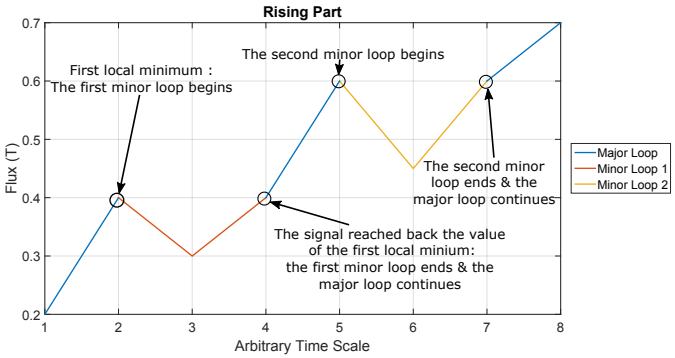


Figure 5: Arbitrary waveform (rising part) split into major and minor loops for core losses calculation

is repeated up to the global maximum. At the global maximum, the falling part begins, and a comparable (albeit inverting local minimums and maximums) procedure starts. The same process is applied to all minor loops to verify the existence of sub-loops. An example of waveform (rising part only) split into major and minor loops is presented in Fig. 5. The core power loss per unit volume is calculated with the equation 4:

$$P_{core} = \sum_i P_{v_i} \frac{T_i}{T} \tag{4}$$

Regarding copper losses, the DC resistance (R_{DC}) of the winding is calculated using their geometry and the resistivity of copper (17 nΩ.m). The joule losses caused by the 50 Hz fundamental frequency can be calculated as $R_{DC} I^2_{rms,LF}$. The calculation of the joule losses for the high frequency ripple require an equivalent AC resistance (R_{AC}), which takes into account skin and proximity effects at the switching frequency. As the distribution of the current in the conductor is affected by the magnetic field in the inductor, there is no analytical expression to calculate R_{AC}. 3D finite elements (COMSOL) simulations are used to calculate the factor K defined as R_{AC}/R_{DC}. The total copper losses are then calculated as:

$$P_{cu} = R_{DC}.(I_{rms,LF} + K.I_{rms,HF})^2 \tag{5}$$

With eq. (5), R_{AC} is assumed to be constant for the fundamental frequency of the current ripple and its harmonics.

The COMSOL model (using version 5.2a) is based on the method described in [9] where each copper track is represented independently to take into account skin and proximity effect. However, the ripple frequency imposes a fine mesh (50 microns elements) on the PCB tracks and on the vias to observe these effects. Using such a fine mesh over the entire geometry would require too much memory, due to the large size of the whole inductor. Instead, the mesh is customized, with different elements size and type for the envelope of the tracks and for the rest of the model, to keep it computationally light. Another solution to keep the computation time low is to simulate the AC resistance for the inductors which belong to the Pareto front only (for the other inductors, a fixed R_{AC}/R_{DC} ratio is considered). The copper loss are calculated with the new R_{AC}/R_{DC} ratio (for the Pareto front inductors only). With

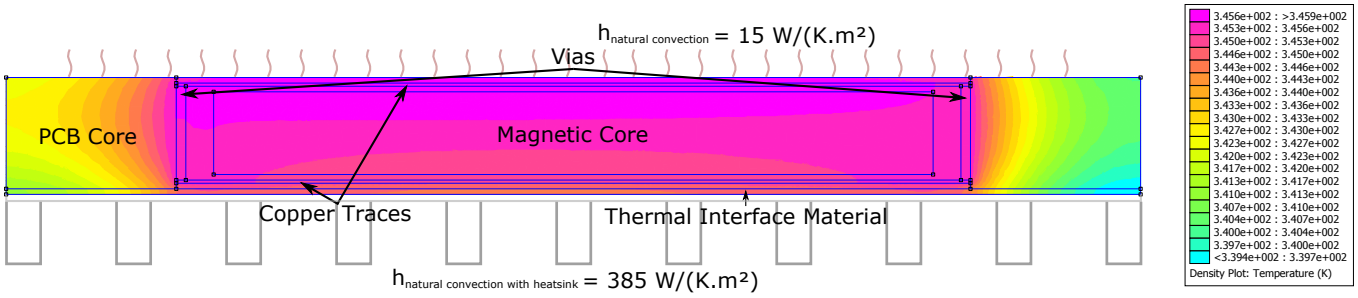


Figure 6: Thermal model for Toroidal PCB design with 3 interleaved PFC cells at 250 kHz and a ripple of 6 A for a Toroidal PCB inductor. On the top surface of the inductor, a heat-exchange coefficient of 15 W/m^{2}K (corresponding to natural convection in air) is considered,. On the bottom surface, we considered a layer of thermal interface material (1.8 °C/W) and a heat-exchange coefficient of 385 W/m^{2}K (corresponding to a heatsink). The ambient temperature is 60 °C.

the new calculated copper losses, the Pareto front may change. In this case, the R_{AC}/R_{DC} is calculated for the new Pareto front inductors. This process continues until the Pareto front remains constant from one iteration to the next.

Thermal Verification:

Once the inductor losses have been calculated, one can estimate the maximum inductor temperature. Here, we consider that the maximum temperature allowed is 100 °C. This limit corresponds to the maximum continuous operating temperature of the PCB (130 °C for ISOLA PCL 370HR), with a safety margin.

The temperature distribution in the inductor is calculated by a finite element simulation using the FEMM software [10]. This software offers the possibility to define the geometry, materials and boundary conditions from the MATLAB command line. However, it is limited to 2D and 2D axi-symmetric simulation. While a 3D model was required to properly simulate the current distribution in the conductors, as presented above, thermal simulations can be performed using a 2D-axi-symetric model. With this simpler model, simulations are much faster (1s per geometry). The thermal model of a Toroidal PCB inductor is presented in Fig. 6, along with the boundary conditions (an equivalent model is built for planar inductors, but it is not shown here due to space constraints). Materials are defined with a thermal conductivity in the r-direction, a thermal conductivity in the z-direction and a volume heat generation density (W/m^3). The last property is used to simulate core and copper losses. When using 2D axial-symmetry, the simulated geometry does not represent exactly the real geometry. In particular, the thermal conductivity of the vias must me homogenized because vias are not fully filled with copper.

In the design procedure described in Fig. 3, a large set of inductor configurations are calculated. From this set, a so-called “Pareto front” is automatically identified in the (losses, box volume) domain: it represents a subset including only the best designs (for any design which does not belong to this Pareto front, it is possible to either find a smaller design with the same losses, or a more efficient design with the same volume).

A thermal model is automatically generated and simulated for each inductor on the Pareto front. The solutions for which the maximum temperature exceeds 100 °C are discarded, and a new Pareto front is calculated. This process is repeated until all inductors on the Pareto front meet the temperature requirement.

III. Designs & Magnetic Material Comparison

The results of the design procedure, for both designs and two magnetic materials are presented in Fig. 7. In each case, these results are represented as a cloud of points (one point per inductor configuration). The best points (low volume, low losses) which offer a maximum temperature of less than 100 °C constitute the Pareto Front. The box dimensions of two examples are given in table III.

Inductor Design	Planar (Green)	Toroidal PCB (Orange)
Magnetic Material	MPP 200	MPP 200
Power Loss (W)	1.21	2.02
Box Volume (cm^3)	8.61	9.10
Box Dimensions (cm^3)	3.3 x 2.9 x 0.9	5.33 x 5.33 x 0.32

Table III: Dimensions for two inductors on the Pareto front (Planar and Toroidal PCB) using MPP200.

From these results, the following conclusions can be drawn:

- The planar structure tends to offer lower losses and lower volume. This is because the maximum allowed thickness for the Toroidal PCB structure tends to results in flat cores with a large diameter, imposing longer copper windings and therefore higher copper losses.
- For the planar structure, many points were removed from the Pareto front, because of the high temperatures reached in the inductor. On the contrary, for the Toroidal PCB structure, the Pareto front follows exactly the bottom boundary of the cloud. This means that the thermal considerations are not a limiting factor for this structure (because of its efficient cooling, due to its large surface).
- With the powder core materials, only a handful of "Toroidal PCB" designs are possible: due to the intrinsic low permeability of these materials, a relatively large number of turns is necessary. Because of the PCB design

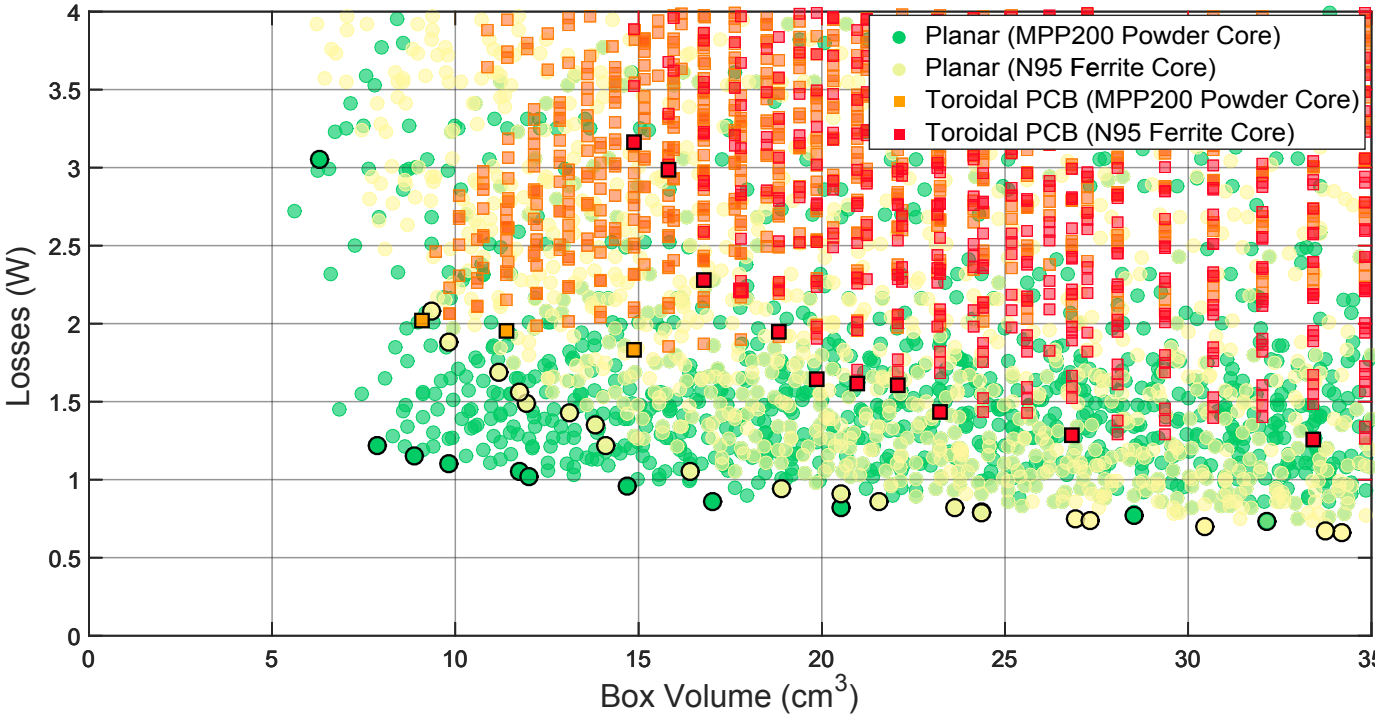


Figure 7: Comparison of the two inductors designs with MPP200 (Powder Core) and N95 (Ferrite Core) for a PFC with 3 cells interleaved, a current ripple of 6 A and a switching frequency of 250 kHz. The Pareto front solutions are highlighted by a black edge.

rules (mainly the size and spacing of the vias), this puts a lower limit on the core inner diameter, and therefore on the box volume. Ferrite materials, which have a much higher permeability, do not suffer from the same limitation.

IV. Conclusion

An automatic procedure was described to design the inductor of a PFC. This procedure starts with the specifications of the inductor, some magnetic materials parameters, and generates a large set of possible designs. From this set, it then identifies the best choices, and uses finite elements models to accurately calculate their performances.

Using this procedure, it was found that the Planar structure, using a powder core, offers the smallest and most efficient solution. But thermal management can be an issue with the smallest inductors. On the contrary, the "Toroidal PCB" structure does not present thermal management issues thanks to its large surface in contact with the heatsink.

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