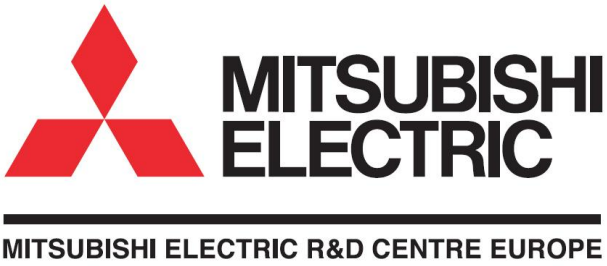


IEEE Energy Conversion Congress and Exposition, Cincinnati, USA, October 2017

DOI: 10.1109/ECCE.2017.8096480

Lifetime Extension of a Multi-die SiC Power Module using Selective Gate Driving with Temperature Feed-forward Compensation

J. Ewanchuk

J. Brandelero

S. Mollov

Lifetime Extension of a Multi-die SiC Power Module using Selective Gate Driving with Temperature Feed-forward Compensation

Jeffrey Ewanchuk, Julio Brandelero, and Stefan Mollov
Power Electronic Systems Division
Mitsubishi Electric Research Centre Europe
Rennes, France
j.ewanchuk@fr.merce.mee.com

***Abstract*— Owing to the high current density but smaller die area of SiC components, high current SiC power modules typically feature a large number of parallel connected dies. Due to the faster electrical dynamics of these power modules, and the inherent mismatch of properties between the dies, certain dies can be poorly utilized – requiring either more dies to achieve a given current rating or a de-rating of the current handling capability of that module. This paper investigates the use of integrated per-die buffers with selective gate driving to minimize the thermal differences within a high current SiC power module. The predetermined selective gate driving pattern is based on the steady-state temperature distribution of the power module, and hence is used as a feed-forward term to compensate the thermal unbalance. The experimental results demonstrate a drop of 15°C in the hottest die using selective gate driving, corresponding to a lifetime increase of up to 3 times, according to the case study presented.**

Keywords—Multi-die power module, gate driver, SiC devices, reliability, thermal control

I. INTRODUCTION

Due to the increasing demand for electrical energy, highly efficient and dense power electronic converters are of increasing importance in the industrial world. Consequently, the increased demands for improved power density require not only more efficient semiconductor components, but also improved utilization of these semiconductors. However, while emerging wide-band gap devices, such as SiC MOSFETs, have increased current densities compared to traditional Si components, large die areas are still uncommon, resulting in a large number of parallel devices required for high current operation [1].

With parallel-connected devices, a number of factors can influence the current distribution from device to device, such as the threshold voltage differences, thermal path differences, and other non-ideal device characteristics [2-5]. As a result, a multi-die power module typically requires a de-rating factor for each die in order to safely operate within a defined power envelope. Thus, research efforts have focused on balancing the current distribution across discrete semiconductor devices, in order to ensure a high utilization of each component within the system [4]. In the case of power modules, substrate layout techniques are largely employed for mitigating the asymmetry in switching behavior [5]. In which case, while switching noise can be minimized, the parallelization of devices still requires matching of threshold voltages to ensure good balanced behavior – thereby increasing the total cost of manufacturing due to screening, and storage.

Thermal balancing or control techniques have been investigated as a means of increasing the power converter lifetime in a number of applications, such as in wind and electric vehicles [6-8]. In general, lifetime extension techniques have involved minimizing the junction temperature swing within the module by a number of techniques, including modulation of the cooling system performance [9], control of the reactive power circulation [7], and variation of the converter switching frequency [10]. Furthermore, the concept of stress steering has been demonstrated for multi-level converters, where the redundant switching states of the converter have been used to ensure balanced thermal loading of the converter, thereby maximizing the total lifetime [8].

This paper investigates the use of integrated per-die gate buffers in a multi-die SiC power module, with selective gate driving, to improve the utilization of the dies within the power module. With the integration of the per-die gate buffers, and the inclusion of a control unit, a more intelligent power module is proposed. Furthermore, while the selective gate driving pattern can be determined based on a number of methods, in this paper it is inspired by the thermal constraints imposed by the geometric layout and electrical characteristics of the power module. Hence, the potential of the proposed scheme is investigated to reduce the peak junction temperature across the parallel set of dies, thereby increasing the lifetime or alternatively, the current rating of the power module.

II. PRINCIPAL OF OPERATION

Considering a single substrate for a multi-die power module, each gate and source connection of the individual dies are typically formed along a bus-bar, as shown in Fig. 1 (a), with a single buffer stage within the gate driver used to provide the energy needed to commutate each device, as shown in Fig. 1 (b). Conversely, as shown in Fig. 2 (a), the

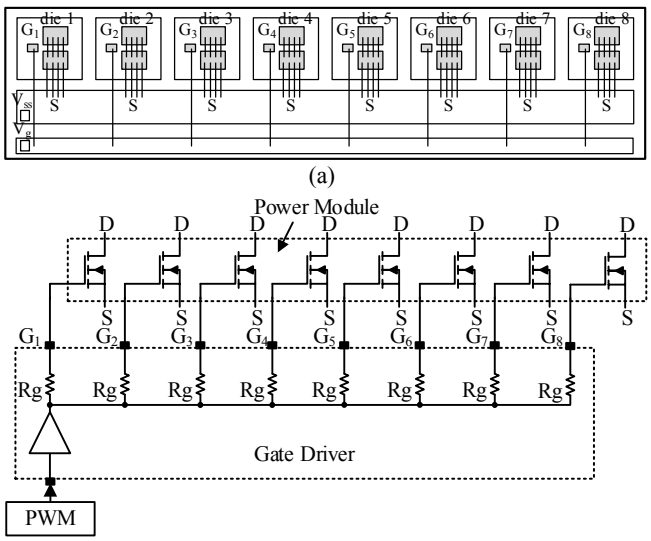


Fig. 1. Standard power module with (a) multi-die arrangement on substrate and (b) logical gate driver arrangement

substrate can be modified to allow individual gate access to each device [5], allowing for a buffer stage to individually control each die, as shown in Fig. 2 (b). This connection to each die minimizes the gate source loop inductance for each die, allowing for faster drain current evolution, and a significant minimization of the switching losses [11, 12]. While individual gate access enables a reduction in total switching losses, a further benefit can be enabled by selectively driving each die independently from one another, as this paper aims to highlight.

Assuming a MOSFET-like device during a switching transient, the drain current is related to the trans-conductance, g_{fs}, gate voltage, $v_{gs}(t)$, and the threshold voltage, V_T, via (1):

$$i_d(t) = g_{fs} \cdot \left(v_{gs}(t) - V_T\right) \quad (1)$$

In this case, with each die in the parallel array having a different trans-conductance, electrical path to the gate, and threshold voltage, it is clear that the evolution of the drain current will not always be identical across the dies during the switching transient – leading to an asymmetry in the switching losses [12, 13]. One possible technique to overcome this limitation is to modify the gate voltage, either in an analog manner to allow synchronous evolution of the drain current during a switching event [3], or in a time-shifted manner, effectively matching the commutation time between devices during a turn-on or turn-off event [4]. However, closed-loop feedback of the drain current or voltage during the commutation is necessary to match the timing between the parallel devices, or to input the correct gate voltage for balanced operation. Hence, while these solutions can be applied to IGBT devices, which feature commutation times on the order of 1-100us, they are generally too slow to be cost-effective to apply to SiC MOSFET power modules, which feature commutation times on the order of 10-100ns.

In this paper, an open loop or feed-forward based selective gate driving pattern is investigated, which employs the re-distribution of switching losses enabled by the per-die buffer architecture – thereby steering the thermal stress within the power module to achieve an increase of lifetime. Therefore, there are several key aspects to the operation of the proposed integrated power module: the re-distribution of switching energy from die to die based on selective gate driving, the relationship between the per-die junction temperature and the input power loss profile, and the derivation of a selective gate driving pattern based on the thermal constraints of the power module, in order to compensate the inherent temperature unbalance within the power module. The implementation of the selective gate driving profile on an FPGA is then described using these thermal constraints as an example, but the selective gate driving pattern can also be developed based on threshold voltage mismatches between the parallel dies, or other constraints affecting the thermal distribution within the power module.

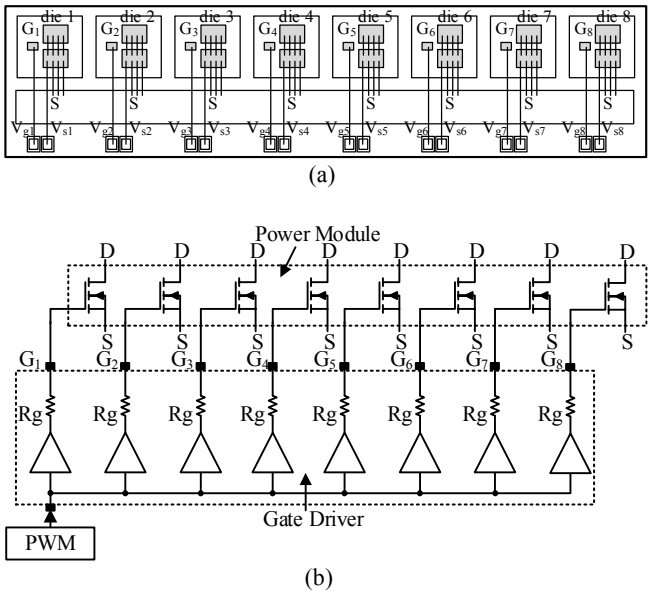


Fig. 2. Power module with 8 dies and per-die buffers (a) multi-die arrangement on substrate and (b) logical gate driver

A. Re-distribution of Switching Energy

In order to manipulate the thermal distribution of individual dies within the power module, a fixed turn on/turn off delay time, t_{delay}, is used to allow one single device to experience nearly zero switching losses, with the neighboring devices assuming the load current for that duration. The die with the selected delay experiences less losses during that switching cycle, thereby allowing a reduction in the temperature of that device. As the delay is fixed in duration, the controller applies action in a discrete manner, and the die temperatures within a module can be selectively targeted.

Practically, during the selective gate driving routine, the neighboring dies see an elevated current for the duration of the delay time, which is related to the number of dies commutating during that instant. In Fig.3 (a), with 'n' dies in parallel sharing a load current of I_d, the neighboring commutating dies assume a proportional amount of current during the delay time, as shown in Fig. 3 (b).

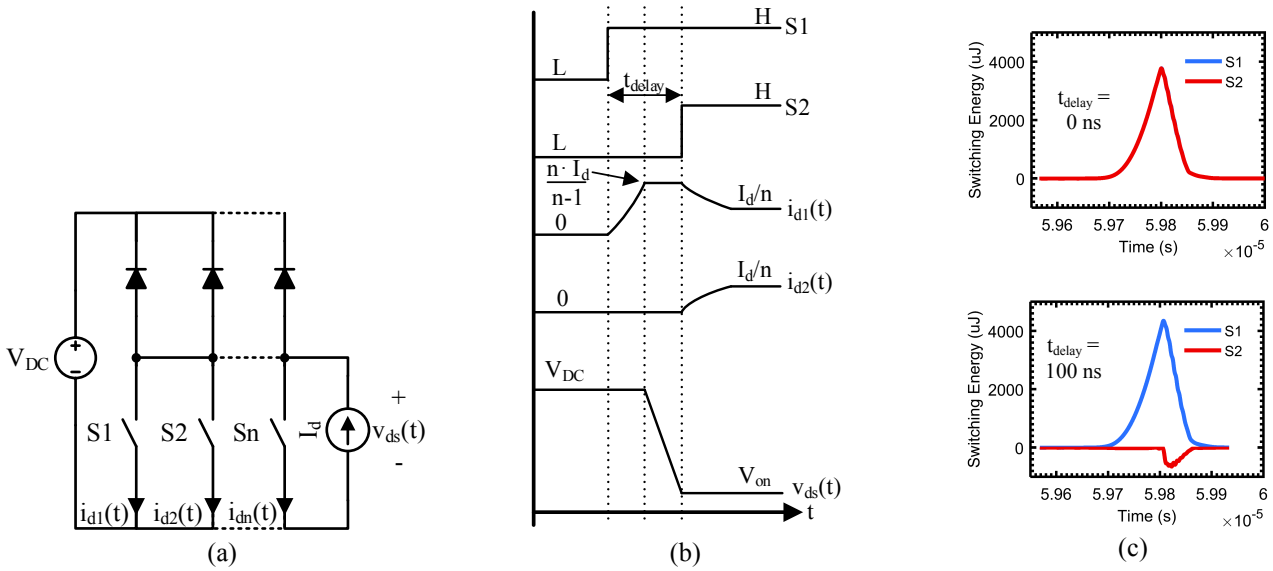


Fig. 3. Mechanism for the re-distribution of switching losses using a fixed time delay in the turn on, turn off of one die (a) example schematic (b) illustration of drain current allocation and (c) simulated switching energies of 8 C2M016012D SiC MOSFETs with one die delayed during turn on and with no delay applied (only two dies shown).

Therefore, the net effect of steering the losses away from a certain die towards the rest of the dies for a single switching cycle is negligible, provided there are sufficient number of dies in parallel. Using a SPICE model of the C2M016012D SiC MOSFET, the selective gate driving action is applied to a single die in Fig. 3 (c), which in turn removes the switching losses of that die. As the neighboring dies have an increase in losses of approximately 8/7 (with 8 dies), the total losses in the module are not affected. Note that the device output capacitances causes some switching activity during the inactive time of the die, and that the delay time is not intended to be applied for every switching cycle.

Although the same selective driving method can be applied to manipulate the conduction losses, it can be shown that for a MOSFET device, it is difficult to reduce the total energy dissipated in the power module due to the inherent current-loss non-linearity. Whereas, if selected correctly, the increased current commutated by the neighboring dies proportionally increases the switching losses, and therefore the average temperature across the set of dies can be maintained. Thus, the selective gate pattern can be applied to re-distribute the switching losses and thereby reduce the peak temperatures in the hottest dies, while increasing the temperature of the coldest dies – allowing the module to dissipate more power losses for a given temperature limit.

B. Approximate Per-die Thermal Model

Assuming that the thermal path from die to the base plate of the power module is largely one-dimensional, and that the base-plate (T_s) has a homogeneous temperature distribution, the equivalent thermal model for each die can be derived, as shown in Fig. 4. To provide context for the selective gate driving pattern, a second-order Cauer thermal model is given in state-space notation, as per (2), with $K \cdot d\hat{x}(t)/dt = A \cdot \hat{x}(t) + B \cdot \hat{u}(t)$, with the die temperature as the state vector, $\hat{x}(t)=[T_1\ T_2 \cdots T_n\ T_s]^T$, and the power losses of each die, $\hat{u}(t)=[P_1\ P_2 \cdots P_n\ \sum P_n]^T$. Solving for the steady-state temperature, the average junction temperature of each die is related to the die input power via (3).

While this closed-form solution can be used as the basis of the selective gate driving pattern, a more general method can be derived to relate the individual junction temperature to the die power losses, where the thermal coupling between dies is non-negligible. In this case, an arbitrary derived thermal impedance network can be defined according to (4), where $R_{x,y}$ refers to the coupled thermal resistance between die 'x' and 'y' – note that in this case, the input power losses and corresponding temperature references are dimensioned according to 'n' dies and does not include the base-plate temperature (T_s) as per (3). The thermal network can then be determined by using the superposition principal via individual device heating in order to characterize the power module [14]. Thus, for the purposes of the selective gate driving pattern, each die can be related to the per-die losses via a derived thermal model.

$$A=\begin{bmatrix} \frac{1}{R_1} & 0 & -\frac{1}{R_1} \\ 0 & \ddots & \vdots \\ 0 & 0 & \frac{1+R_s}{R_s}\cdot\frac{\Sigma R_n}{\Pi R_n} \end{bmatrix} \quad B=\begin{bmatrix} -1 \\ \vdots \\ -1 \end{bmatrix} \quad K=\begin{bmatrix} C_1 & 0 & 0 \\ 0 & \ddots & 0 \\ 0 & 0 & C_s \end{bmatrix} \tag{2}$$

$$\begin{bmatrix} T_1 \\ \vdots \\ T_n \\ T_s \end{bmatrix}=\begin{bmatrix} R_1 & \cdots & \frac{R_s}{1+R_s}\cdot\frac{\Pi R_n}{\Sigma R_n} \\ 0 & \ddots & \vdots \\ 0 & \cdots & \frac{R_s}{1+R_s}\cdot\frac{\Pi R_n}{\Sigma R_n} \end{bmatrix}\cdot\begin{bmatrix} P_1 \\ \vdots \\ P_n \\ \Sigma P_n \end{bmatrix}+T_{amb} \tag{3}$$

$$\begin{bmatrix} T_1 \\ \vdots \\ T_n \end{bmatrix}=\begin{bmatrix} R_1 & \cdots & R_{1,n} \\ \vdots & \ddots & \vdots \\ R_{n,1} & \cdots & R_{n,n} \end{bmatrix}\cdot\begin{bmatrix} P_1 \\ \vdots \\ P_n \end{bmatrix}+T_{amb} \tag{4}$$

C. Temperature Feed-forward Compensation Calculation

Using a fixed delay time to manipulate the switching losses for a specific die, it is clear that a target input power $[P_1 \cdots P_n]^T$ can be formed to match a target temperature profile $[T_1 \cdots T_n]^T$ based on (4) or (3). Hence, assuming only one die is delayed for a given switching period, a thermal duty cycle, α_i, can be defined for die '*i*'. The thermal duty cycle is the ratio between the number of switching cycles where the fixed delay is applied to a given die and the total number of cycles in the switching pattern – with the sum of all duty cycles inferior or equal to 1. The per-unit time spent at normal operation (i.e. with no selective delay active) is defined as α_0, according to (5), and it represents an independent variable with which to adjust the intensity of intervention with selective gate driving.

$$\alpha_0 = 1 - \sum_{i=1}^{n} \alpha_i \tag{5}$$

Consequently, assuming that the presence of a delay time removes the switching losses in the target device to approximately zero, the power loss profile can be represented as (6), where $P_{sw,i,j}$ is defined as the switching losses of die 'i' with die 'j' held inactive for the switching transition, $P_{sw,i,0}$ is defined as the switching losses of die 'i' at normal operation and $P_{cond,i}$ is the conduction losses for die 'i'. Note that as mentioned in Section II. A, the increase of switching losses in the active dies due to the inactivity of die 'i' can be linearly approximated by number of dies, and hence, for example, the vector $\left[P_{sw,1,1} \cdots P_{sw,n,1}\right]^T = \left[0 \ \frac{n}{n-1} \cdot P_{sw,n,0} \cdots \frac{n}{n-1} \cdot P_{sw,n,0}\right]^T$. The feed-forward vector used to selectively drive each gate according to the target temperature profile, can be defined by solving (4) and (6) for $[\alpha_1 \cdots \alpha_n]^T$ either directly or iteratively.

$$\begin{bmatrix} P_1 \\ \vdots \\ P_n \end{bmatrix} = \begin{bmatrix} P_{sw,1,1} - P_{sw1,0} & \cdots & P_{sw,1,n} - P_{sw,1,0} \\ \vdots & \ddots & \vdots \\ P_{sw,n,1} - P_{sw,n,0} & \cdots & P_{sw,n,n} - P_{sw,n,0} \end{bmatrix} \cdot \begin{bmatrix} \alpha_1 \\ \vdots \\ \alpha_n \end{bmatrix} + \begin{bmatrix} P_{sw,1,0} + P_{cond,1} \\ \vdots \\ P_{sw,n,0} + P_{cond,n} \end{bmatrix} \tag{6}$$

D. Implementation of the Feed-forward Compensation

With the selective gate driving pattern established based on the steady state thermal network of the power module, an FPGA is used to provide the logic for the individual gates in the power module. In brief, an external pulse width modulation signal (PWM) is applied to the input terminal of the power module, and the FPGA captures the edge transitions of this input signal, translating it to each gate buffer, as shown in Fig. 5 (a). Hence, from the input PWM signal, the FPGA modifies the gate pulses for each individual die, based on the pre-programmed pattern bias, $[\alpha_1 \cdots \alpha_n]^T$ to achieve an objective power profile and consequent temperature profile.

As pattern bias represents the duration at which die 'i' is delayed, according to a selected time base, T_B, a counter is used to sequence each die delay period, as shown in Fig. 5 (b). During each identified segment, the output of the counter is used to select which die is delayed, and which dies are unaffected during that duration. Hence, as the counter passes through the segments identified by the pattern bias, each

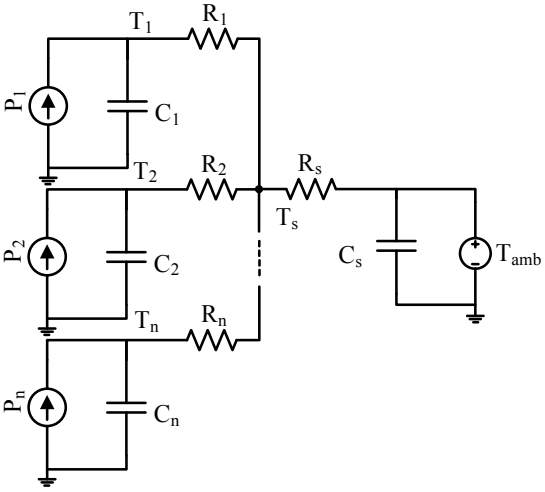


Fig. 4. Second order Cauer Thermal Representation of the Power Module

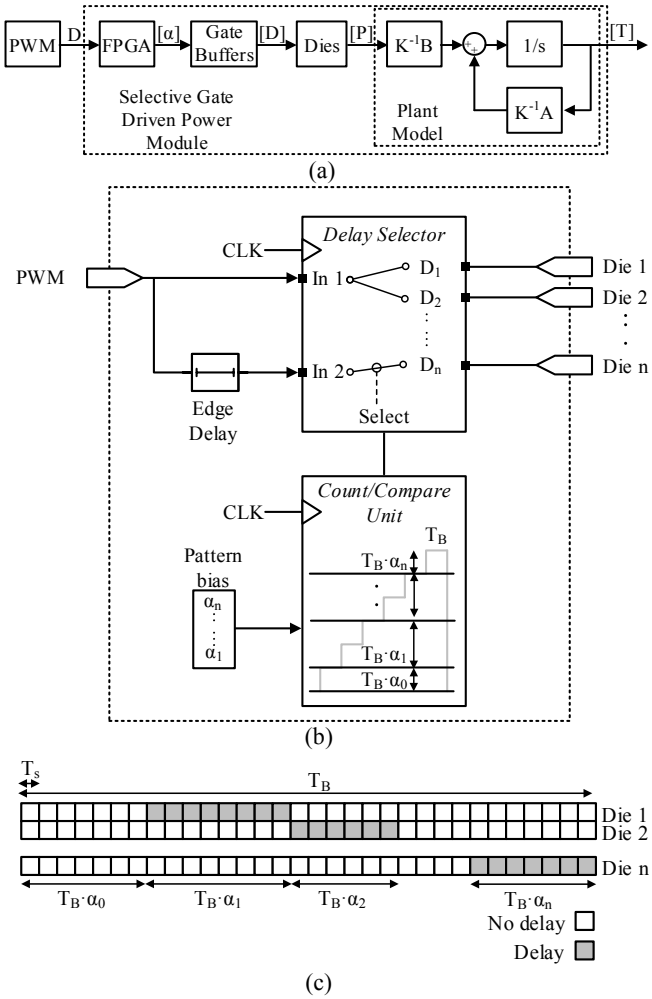
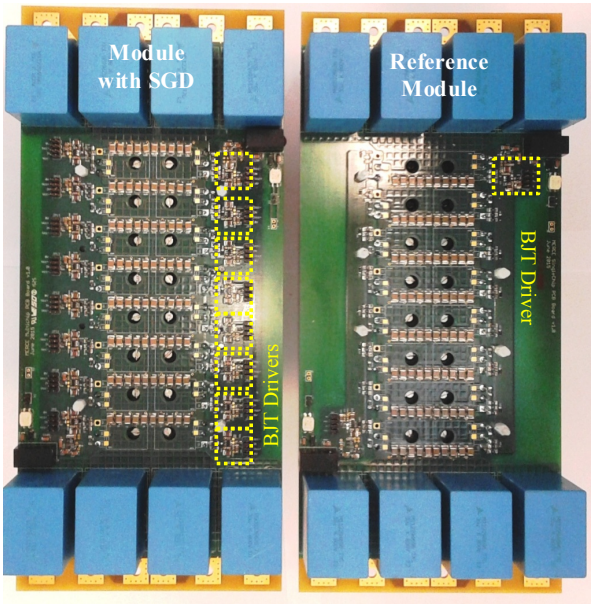
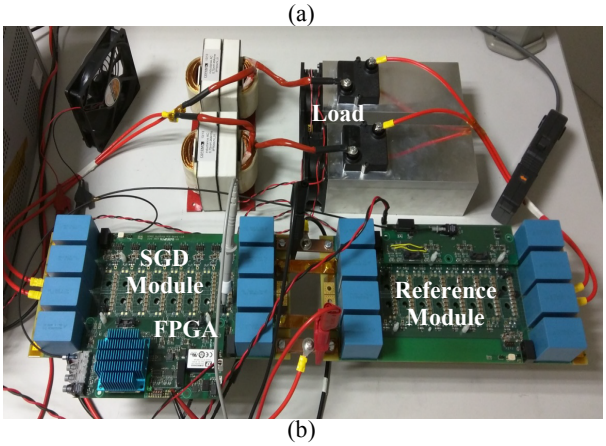


Fig. 5. Implementation of the feed-forward compensation a) block diagram of individual gate control b) FPGA controller implementation c) Time diagram of the die passivation



(a)



(b)

Fig. 6. 1.2kV, 50A discrete prototype with 8 parallel C2M016012D SiC MOSFETs where SGD denotes Selective Gate Driving

successive die is delayed according to the duration identified in the pattern bias, as shown in Fig. 5 (c). Thus, from the pattern bias, the selective gate driving is performed by a simple FPGA implementation.

III. Experimental Results

In order to validate the proposed selective gate driving technique for an integrated power module, a mock power module was developed using 8 parallel C2M0160120D discrete SiC MOSFETs, as shown in Fig. 6 (a), and set in a back-to-back configuration to load the module under rated conditions, as shown in Fig. 6 (b). In order to ensure switching loss linearity during the operation (or less than 5% deviation) of the proposed method, the system was designed to operate with a peak output current of 50A at 1.2kV. With the prototype shown in Fig. 6, an infrared thermal camera was used to determine the thermal resistance model, as shown in (7), by selectively applying current to each device, and monitoring the resulting die temperature distribution [14]. While this method is adequate for determining the junction to ambient thermal resistance of each device, the device to device thermal resistance was significantly impacted by the accuracy of the thermal camera, limiting the error to approximately 6%.

$$R_{th} = \begin{bmatrix} 1.37 & 0.21 & 0.17 & 0.15 & 0.11 & 0.12 & 0.1 & 0.11 \\ 0.21 & 1.33 & 0.22 & 0.17 & 0.12 & 0.12 & 0.1 & 0.12 \\ 0.16 & 0.19 & 1.49 & 0.21 & 0.14 & 0.13 & 0.11 & 0.12 \\ 0.13 & 0.14 & 0.23 & 1.33 & 0.18 & 0.16 & 0.12 & 0.13 \\ 0.11 & 0.11 & 0.15 & 0.22 & 1.3 & 0.2 & 0.14 & 0.15 \\ 0.1 & 0.1 & 0.13 & 0.16 & 0.18 & 1.33 & 0.18 & 0.17 \\ 0.09 & 0.08 & 0.11 & 0.13 & 0.14 & 0.2 & 1.31 & 0.22 \\ 0.08 & 0.08 & 0.1 & 0.12 & 0.11 & 0.16 & 0.22 & 1.41 \end{bmatrix} \quad (7)$$

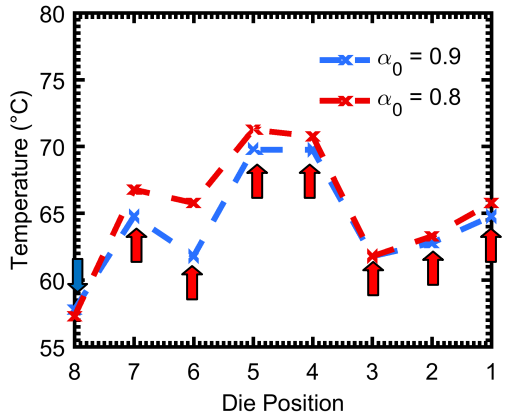
Allowing for further comparison, the entire experimental setup consists of one power module using selective gate driving, i.e. Fig. 2 (b), and another using a gate driver with a single buffer, i.e. Fig. 1 (b), termed the reference power module. These two modules are depicted in Fig. 6 (a), with the integrated gate buffers highlighted. All experimental results are taken under a condition of V_{DC} = 600 V, I_{out} = 50 A with a switching frequency of f_c = 200 kHz. Die 8 refers to the die closest to the fan on the SGD module, but the furthest away from the fan on the reference module.

To illustrate the effect of the delay time being applied to a single die, consider Figs. 7 (a) and (b), where dies 8 and 5 are delayed during 10% and 20% of the operation time. Increasing the number of switching cycles where die 8, is inactive results in a temperature increase of the rest of the dies, but only a minor decrease in the temperature of die 8. Conversely, increasing the number of switching cycles where die 5 is delayed results in a decreasing temperature of that die, but an increase of the hottest die temperature (die 4). Hence, selective gate driving pattern must be determined by considering the entire system in order to have any tangible benefit. .

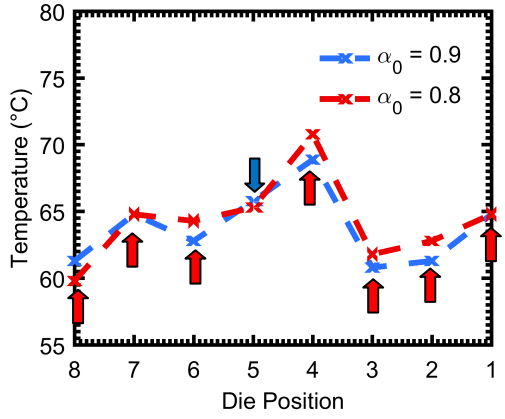
Considering the entire set of devices and fitting for a target temperature rise of 45°C above ambient, the feed-forward vector was determined to be $\alpha = [0.047, 0, 0, 0.243, 0.215, 0, 0.194, 0]^T$ with $\alpha_0 = 0.7$ and $= [0.055, 0, 0, 0.192, 0.165, 0, 0.143, 0]^T$ when $\alpha_0 = 0.5$. Consequently, the effect of these selective driving profiles can be seen in Fig. 8, contrasted against no intervention ($\alpha_0 = 1$), and the reference power module. While the increasing intervention activity clearly decreases the peak junction temperature of the hottest die from 72°C to 67°C, the lowest temperature also increases accordingly – indicating a better utilization of the set of devices as a whole.

IV. Discussion

In order to illustrate the influence of the selective gate driving profile on the extension of the lifetime for the integrated power module, the action over the lifetime of the power module must be considered over that of a given operation instance. As an illustrative case study based on the experimental results obtained in Fig. 8, a simulation is developed where the two considered power modules are loaded according to the usage defined in a “New European Driving Cycle” mission profile [15]. In the reference



(a)



(b)

Fig. 7. Effect of selectively driving a single device on the device temperature with a per-unit intevention time for (a) die 8 and (b) die 5

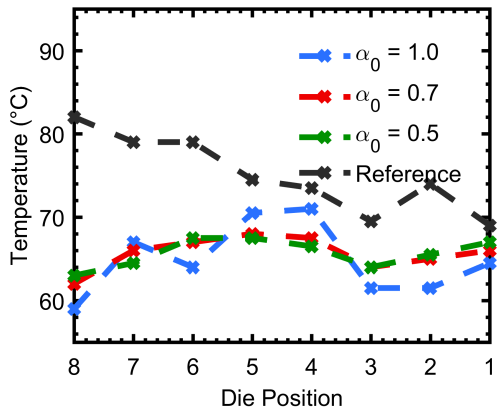


Fig. 8. Temperature profile for the set of dies according to the pre-calculated feed-forward term with an increasing per-unit intervention time and profile for the reference module

power module, the hottest and coldest dies are determined based on their difference in thermal resistance, and the corresponding temperature profile over time is given in Fig. 9. As can be seen from Fig. 9, the hottest die clearly experiences higher amplitude temperature fluctuations, i.e. ΔT_j, when compared to the coldest die in the reference module.

Applying a counting technique, such as the Rain-flow counting method [16], the junction temperature profiles of Fig. 9 can be decomposed into the number of temperature excursions. The damage from each successive temperature excursion can then be estimated by employing the Palmgren-Miner's rule [17], and a wear-out based lifetime model, i.e. a simplified version of Bayerer's model, where β_1= -4.416, β_2=1285,β_3=-0.463 and A=9.3e14 [18], according to (8). Similar approaches to lifetime estimation have been described for power converters subjected to complex loading profiles in wind applications [19].

$$N_f = A \cdot (\Delta T_j)^{\beta_1} \exp\left(\frac{\beta_2}{T_{jmin}}\right) \cdot t_{on}^{\beta_3} \qquad (8)$$

Thus, each temperature excursion is translated to a specific amount of damage, and the total amount of damage can be summed for each respective temperature profile for both the hottest and coldest die. Assuming that the mission profile repeats until failure, the damage until the normalized end of life, where the damage is equal to unity, is expressed as a function of the normalized cycles to failure, as shown in Fig. 10. Comparing the end-of-life for the hottest die against the coldest die, the estimated lifetime differs by a factor of approximately 3. As these dies form a single switch in the power module, the overall lifetime is limited by the weakest die, and hence, the lifetime of the power module will be close to that of the hottest die.

Considering the application of the selectively driven power module against the reference power module, the addition of the individual gate buffers doubles the lifetime, as shown in Fig. 10 with α_0=1. This result corresponds to the peak temperature reduction illustrated in Fig. 8, where the selectively driven module decreases the hottest die temperature from 82°C to 72°C, and is a consequence of minimizing and decoupling the parasitic source inductance for each die [12]. Applying the pattern bias with α_0=0.5, as described in Section V, the temperature is more equally shared between the dies, resulting in an improvement of the normalized lifetime by a factor of 50% compared to the case without a pre-determined selective gate pattern.

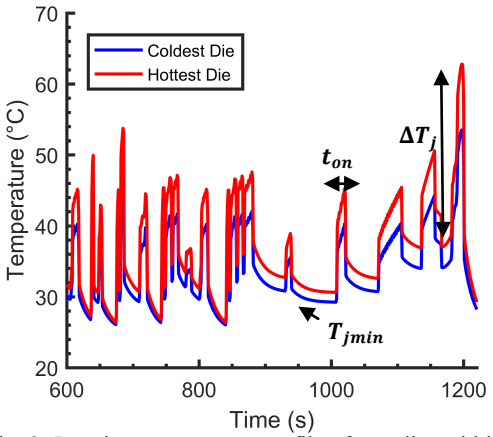


Fig. 9. Junction temperature profile of two dies within the reference power module loaded by a NEDC mission profile

When compared to the reference module, the lifetime has improved by a factor of nearly 3, or nearly the same as the lifetime determined by the coldest die in the reference module. Furthermore, if the profile contained more severe usage, the lifetime could be increased by larger factor due to the larger temperature fluctuations. Thus, by applying a selective gate pattern, the peak temperatures across the power module can be balanced, and the lifetime extended.

Alternatively, for the presented experimental system described in Section V, the selectively driven power module has a 15°C margin to accommodate additional losses (approximately 50%) compared to the reference power module. Consequently, for the same rated peak junction temperature of the semiconductors, the conducted load current can be increased by a factor of 20% - thereby improving the power density of the module. Thus, by improving the die utilization within the power module, the lifetime of the power module can either increase or cope with a higher current density for the same area.

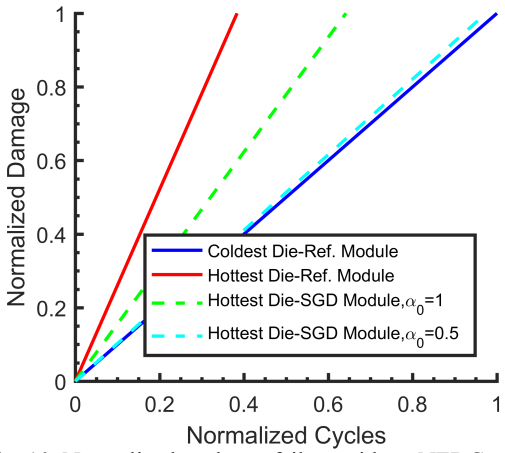


Fig. 10. Normalized cycles to failure with an NEDC mission profile for the reference module, with the hottest and coldest dies illustrated (solid lines), and the selectively driven power module, with increasing intervention time (dashed lines).

V. CONCLUSION

In this paper, the benefits of using an integrated gate driver with a per-die buffer design and selective gate driving for multi-die SiC MOSFET power modules was considered from the perspective of increasing the die utilization. It was shown that the peak junction temperature of a set of devices can be reduced by applying a feed-forward pattern to selectively alter the switching loss profile within the target power module. Based on the thermal constraints of the power module in steady-state operation, a pattern was derived and the implementation was described on a FPGA. The experimental results confirm a 15°C reduction in peak junction temperature for the hottest die of the integrated power module when compared to a referece power module design, and consequences of this reduction of temperature was presented based on a lifetime estimation technique. Thus, using selective gate driving on an integrated power module can improve the utilization of the dies, and consequently extend the lifetime of the power module or improve the current density of that module.

Further work considers a closed-loop approach that effectively responds to a degrading and aging die thermal interfaces.

REFERENCES

[1] R. Roesner, “LV5+ - SiC MegaWatt PV Inverter” ECPE SiC & GaN Forum, Potential of Wide Bandgap Semiconductors in Power Electronic Applications, March 2017

[2] H. Li *et al.*, "Influences of Device and Circuit Mismatches on Paralleling Silicon Carbide MOSFETs," in IEEE Trans.on Power Elect., vol. 31, no. 1, pp. 621-634, Jan. 2016.

[3] X. Wang, Z. Zhao and L. Yuan,"Current sharing of IGBT modules in parallel with thermal imbalance," 2010 IEEE ECCE, Atlanta, USA

[4] R. Alvarez and S. Bernet, "A new delay time compensation principle for parallel connected IGBTs," 2011 IEEE ECCE, Phoenix, USA

[5] H. Li, S. Munk-Nielsen, S. Bęczkowski and X. Wang, "A Novel DBC Layout for Current Imbalance Mitigation in SiC MOSFET Multichip Power Modules," in IEEE Trans. on Power Elect., vol. 31, no. 12, pp. 8042-8045, Dec. 2016.

[6] M. Andresen, M. Liserre and G. Buticchi, "Review of active thermal and lifetime control techniques for power electronic modules," EPE 2014, Lappeenranta, Finland.

[7] D. Zhou, F. Blaabjerg, M. Lau and M. Tonnes, "Thermal Behavior Optimization in Multi-MW Wind Power Converter by Reactive Power Circulation," in IEEE Trans. on Industry Appl., vol. 50, no. 1, pp. 433-440, Jan.-Feb. 2014.

[8] K. Ma and F. Blaabjerg, "Thermal optimised modulation methods of three-level neutral-point-clamped inverter for 10 MW wind turbines under low-voltage ride through," in IET Power Electronics, vol. 5, no. 6, pp. 920-927, July 2012.

[9] D. A. Murdock, J. E. R. Torres, J. J. Connors and R. D. Lorenz, "Active thermal control of power electronic modules," in IEEE Transactions on Industry Applications, vol. 42, no. 2, pp. 552-558, March-April 2006.

[10] L. Wei, J. McGuire and R. A. Lukaszewski, "Analysis of PWM Frequency Control to Improve the Lifetime of PWM Inverter," in IEEE Trans. on Industry Appl., vol. 47, no. 2, pp. 922-929, March-April 2011

[11] Semikron IGBT Module SEMiX606GAR066HD

[12] J. Ewanchuk, J. Brandelero, S. Mollov, “Improving the Die Utilization and Lifetime ina Multi-die SiC Power Module by means of Intergrated Per-die Gate Buffers” ISPSD 2017, Sapporo, Japan

[13] J. Colmenares, D. Peftitsis, H. P. Nee and J. Rabkowski, "Switching performance of parallel-connected power modules with SiC MOSFETs," 2014 ECCE ASIA, Hiroshima, Japan

[14] P. Dubus, R. Leon, D. Le Guyader and L. Caves, "Thermal pre-dimensioning methodology based on thermal impedance," 2010 CIPS, Nuremberg, Germany

[15] Department of Transport, “Vehicle Emissions Testing Programme”, 2016. [Online]. Available: https://www.gov.uk/government/uploads/system/uploads/attachment_data/file/548148/vehicle-emissions-testing-programme-web.pdf [Accessed: 26-Jun-2017]

[16] M. Matsuishi, T. Endo, “Fatigue of Metals Subjected to Varying Stress”, Japan Soc. Mech. Engineering, 1968.

[17] M.A. Miner, “Cumulative damage in fatigue,” J. Appl. Mech., vol. 12, pp. A159–A164, 1945

[18] K. Ma, M. Liserre, F. Blaabjerg and T. Kerekes, "Thermal Loading and Lifetime Estimation for Power Device Considering Mission Profiles in Wind Power Converter," in IEEE Transactions on Power Electronics, vol. 30, no. 2, pp. 590-602, Feb. 2015.

[19] R. Bayerer, T. Herrmann, T. Licht, J. Lutz and M. Feller "Model for Power Cycling lifetime of IGBT Modules - various factors influencing lifetime," 2008 CIPS, Nuremberg, Germany