Topological and Device Cost-Performance Optimization for 3-Phase Inverters in High Speed Electric Drive Systems

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Abstract

As new semiconductors push the boundaries in terms of switching speed and power density, the packaging must also adapt to fully exploit the gains possible with emerging devices. In order to minimize die costs associated with these emerging devices, a 3-level mixed Si/SiC topology is compared against a 2-level all-SiC topology in order to reduce the number of high cost SiC dies used to construct a liquid cooled module intended for 3-phase high speed electric drive systems. It is found that while the 3-level mixed Si/SiC topology can reduce the required number of SiC dies, the 2-level all-SiC topology remains advantageous due to the limited switching frequency considered.

Keywords: Multi-level Converters, Cost, Parallel SiC dies, High Speed Electric Drive

INTRODUCTION

New module packaging technologies can fully exploit the advances in wideband gap devices (e.g. SiC) by not only reducing parasitic path inductances, but also by decreasing thermal impedances and thereby improving the heat transfer capability for a given module [1]. With these new packaging technologies, power densities can further increase over that of the current generation. However, the utilization of SiC components in these packages remains costly due to the high number of dies required to achieve high power levels.

However, with a given dc voltage, 3-level dc/ac topologies have been shown to reduce semiconductor die areas by better utilization of the devices [2, 3]. In particular, by employing a switched neutral, the 3-level T-type converter reduces the current stress within the high voltage rated devices of the topology [3].

Therefore, considering the high density power module of Figure 1, this paper compares the die costs associated with a 2-level all-SiC converter, shown in Figure 2, against a 3-level converter, shown in Figure 3, that uses low cost Si devices to reduce the constraints on the higher cost SiC devices. Assuming application in a three-phase high-speed electric drive system, the minimum number of SiC MOSFET dies required for each topology is calculated from a thermal model of the liquid cooled module under identical power loading conditions.

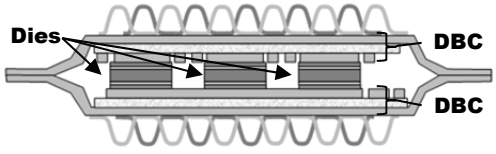

Figure 1. 3-phase liquid-submersed module with direct and double-sided cooling with side-view slide of single phase leg

METHODOLOGY

This section details the methodology used to compare the number of parallel connected SiC dies required by each topology to produce an understanding of the die related costs.

Assuming a 700V dc bus, the converter circuit is designed to provide 70kW peak output power (P_{out}), under a lagging power factor of 0.8 at a fundamental frequency of 500 Hz – a typical operating condition at high rotational speeds. Due to the high fundamental frequency, a switching frequency of 20 kHz (f_c) is targeted as a compromise between controller implementation performance and current harmonic distortion. Thus, under the assumption of the latter parameters, a simulation model is developed that incorporates the switching and conduction losses at the die level for each topology. However, due to the coupling between the number of dies, the static and dynamic

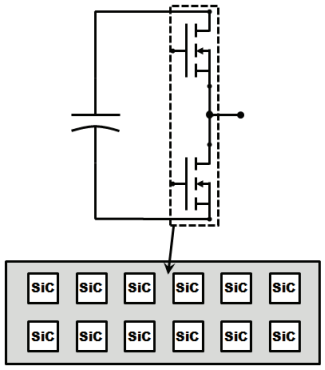

Figure 2. Phase leg arrangement of the 2-level converter (2-L) with 6 parallel SiC MOSFET dies per device

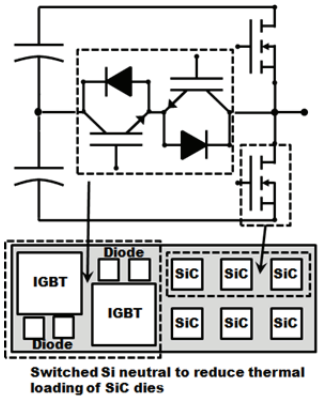

Figure 3. Phase leg arrangement of the 3-level switched neutral converter (3-L SN) with 3 parallel SiC dies per MOSFET device

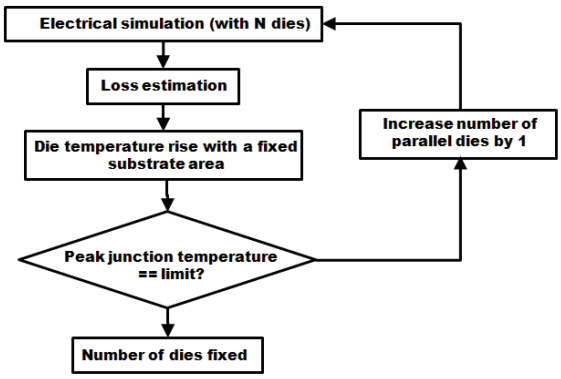

Figure 4. Methodology to compare the two proposed topologies for integration in the module illustrated in Figure 1 by iterating through the number of parallel SiC MOSFET dies.

losses and the thermal constraints of the converter, a recursive methodology is employed to calculate the minimum dies required, i.e. as shown in Figure 4. Therefore, in order to evaluate the two candidate topologies, two stages are necessary: estimation of switching and conduction losses per device in each topology, and the required number of dies via the thermal model of the liquid cooled power module.

A. Estimation of Losses

With an initial number of parallel SiC dies, a PSIM simulation estimates loss per die, based on the methodology developed in [6, 7], in both forward and regenerative mode using synchronous rectification for the SiC MOSFETs. In brief, the simulation model uses an ideal device for interaction with the load, but the instantaneous currents and voltages at each time step are used in a device loss model, derived from the associated data sheet. The device is therefore represented by the static characteristics and the dynamic characteristics per die as a function of current and voltage. A simplification of the estimation of the losses is illustrated in Figure 5. The electrical machine is modelled by resistive-inductive impedance behind a three-phase voltage source – with the phase inductance chosen to limit the phase ripple current to 10% of the phase current magnitude. The forward or regeneration model is then produced via phase shifting the emulated machine voltage relative to the applied voltage. Lastly, each converter is pulse-width modulated using sinusoidal pulse-width modulation with third harmonic injection to improve bus utilization.

The parameters used in the estimation of each device are summarized in Table I. The static characteristics were estimated from the die datasheets but due to the lack of dynamic characteristic information at the die level, an estimate is obtained via switching energy curves from the datasheets of similarly rated discrete devices/modules. As each topology should withstand a 700V dc bus voltage, the 2-level converter is composed of 1.2kV SiC MOSFETs from CREE [4], whereas the 3-level T-type converter is composed of the same MOSFETs for the 'main' leg, and 600V IGBT devices from Infineon [5] with 650V SiC SB diodes from CREE on the 'auxiliary' neutral switch. In order to estimate the switching losses, the total switching energy is scaled as function of the current, and by the blocking voltage. Lastly, as the objective is

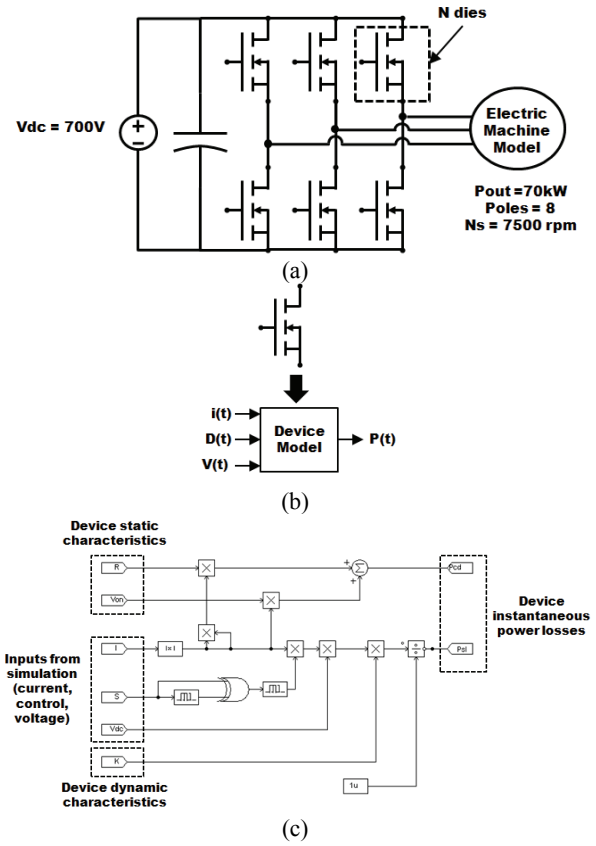

Figure 5. Instantaneous device power loss prediction based on [6,7] with (a) high level simulation with load assuming the 2-level converter, (b) SiC MOSFET device representation and (c) loss model relationship

1.2kV SiC MOSFET	
Die (static)	*CMF-1200-S080D*
Die area	*16mm²*
Rds(on) @ 125C	*125mΩ*
K_{loss} (mJ/A)	*8e-5·I²-2e-3·I+0.0375 (est.)*
600V IGBT	
Die (static)	*SIGC54T60R3*
Die area	*53mm²*
Rce(on) @ 125C	*25mΩ (est.)*
Vce(on) @ 100A	*1.45V*
K(mJ/A)	*3e-7·I²-2e-4·I+0.0768 (est.)*
650V SiC SBD	
Die (static)	*CPW2-0650-S010B*
Die area	*4mm²*
V_F(on)@10A/175C	*2V*
Q_C (@ 500A/us)	*15nC*

Table 1: Specification of Devices used to Estimate Losses

to determine the minimum number of dies, the junction temperature of each device is limited to 125°C and this temperature is used in the estimation of the thermally dependant losses [6, 7].

B. Calculation of Die Temperature Rise

The estimated power losses per die from the electrical simulation are transferred to a heat flux – i.e. the losses over the die area, which is then translated to a temperature rise using a Fourier series solution to model the thermal loading within the module. Other analytical thermal modelling solutions could

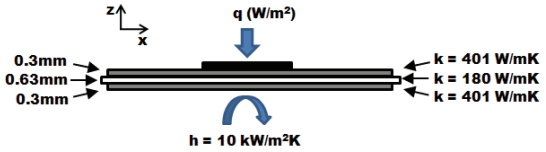

Figure 6. Simplified heat path of die to cooling interface with AlN substate and double sided cooling of the module depicted in Figure 1 (simplified to equivalent single heat path)

have been implemented, i.e. 45° approximation for heat spreading, but the latter method suffers from poor accuracy with the thermal properties of the power module considered in Figure 6 [8].

The module in Figure 1 is modelled by simplified the heat path illustrated in Figure 6. In this approach, an AlN substrate from Curamik [9] is selected with a maximum dimension of 13.8cm by 19.1cm. The heat path is simplified to a single convection co-efficient of 10kW/m^{2}K – which is a typical value for double sided cooled modules, i.e. [10]. However, due to the multi-material substrate, the thermal conductivity is simplified to a single equivalent value of 282 W/mK with a thickness of 1.26mm, via [13-15]. In the latter procedure, a single die is assumed to be in the centre of a 15mm by 15mm 3-layer substrate, with the thermal conductivity coefficients defined in Figure 6.

The thermal distribution of the dies on each substrate is estimated by using a 2D Fourier series solution developed for convection cooled plates with discrete heat sources [12, 15]. In brief, while the temperature distribution within the module is a 3D problem, a 2D temperature distribution is produced by considering the solution for only the top layer of the substrate [12, 15]. As such, the X by Y substrate is segmented into N and M lengths, as per (1), where both of these dimensions are much greater than the substrate thickness. Each heat source (e.g. a power die) is located at a point in the substrate on the (x,y) plane, with the physical dimensions defined by x_2 and x_1, by y_2 and y_1, as depicted in Figure 7. The numbers of points that compose the substrate are defined by the limit in (1), with a number selected with computational time in consideration.

$$N > \frac{3X}{x_2 - x_1}, M > \frac{3Y}{y_2 - y_1} \tag{1}$$

Using a mathematical software tool, e.g. MATLAB, a script is developed to iterate through the segmented substrate of 'M' and 'N' points, and evaluates the thermal solution at each of these points [6]. Therefore, along one axis, (2) is calculated, based on the number of points in the orthogonal axis:

$$f(n,y) = \sum_{m}^{M} B_{mn} \cdot \cos(m \cdot \omega_y \cdot y) \tag{2}$$

$$\text{Where, } B_{0n} = \frac{\omega_y \cdot (y_2 - y_1)}{\pi \left[\left(\frac{n \cdot \omega_x}{\kappa} \right)^2 + 1 \right]}, \text{ m=0} \tag{3}$$

$$B_{mn} = \frac{2\left[\sin(n \cdot \omega_y \cdot y_2) - \sin(n \cdot \omega_y \cdot y_1)\right]}{m\pi \left[\left(\frac{n \cdot \omega_x}{\kappa} \right)^2 + \left(\frac{m \cdot \omega_y}{\kappa} \right)^2 + 1 \right]}, \text{ m>0} \tag{4}$$

Relative to the ambient temperature, each point on the substrate therefore has the temperature defined via (5) for each new loop along the orthogonal axis:

$$\vartheta(x,y) = \frac{\gamma}{\kappa^2} \cdot \sum_{n=0}^{N} f(n,y) \cdot A_n \cdot \cos(n \cdot \omega_X \cdot x) \tag{5}$$

$$\text{Where, } A_0 = \frac{\omega_X \cdot (x_2 - x_1)}{\pi}, \text{ n=0} \tag{6}$$

$$A_n = \frac{2\left[\sin(n \cdot \omega_X \cdot x_2) - \sin(n \cdot \omega_X \cdot x_1)\right]}{n\pi}, \text{ n>0} \tag{7}$$

The constants used in the iteration loop are defined via (8), where 'q' is the heat-flux (W/m^2), 'k' is the thermal conductivity (W/mK), 'δ' is the substrate thickness (m), and 'h' is the convention coefficient (W/m^{2}K):

$$\gamma = \frac{q}{k \cdot \delta}, \kappa = \sqrt{\frac{2 \cdot h}{k \cdot \delta}}, \omega_x = \frac{\pi}{B}, \omega_y = \frac{\pi}{H} \tag{8}$$

With (1)-(8) developed for a single power die across a substrate of X and Y dimension, the total temperature distribution with more than one die is a sum of each the solutions calculated via the superposition theorem [12]. Therefore, with the power module modelled with an arbitrary number of dies, the losses are calculated via Section A, and the temperature rise over the substrate is given via (1-8) for each die.

To confirm the thermal prediction accuracy of the approach for a single die described as per (1)-(8), the power module is modelled via FEMM [11], and compared assuming an infinite plane in the y-axis. Considering the top copper layer of the substrate with a thin power die, the thermal distribution of the die on the substrate is depicted in Figure 8. Thus, from Figure 8, the methodology described as per (1)-(8) produces a thermal distribution within reasonable accuracy compared to the finite element solution (slightly lower peak temperature value), and therefore valid to use as a basis of comparison to determine the individual thermal loading per die.

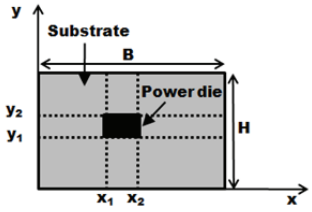

Figure 7. Temperature distribution on a substrate over the (x,y) plane from discrete rectangular heat sources, e.g. power dies, as described in [12, 15].

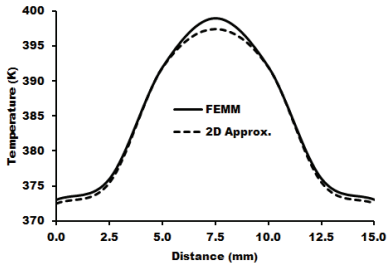

Figure 8. Thermal distribution on the top copper layer of a 15mm

THERMAL CHARACTERIZATION OF TOPOLOGIES

In this section, the 2-level all-SiC solution is compared against the mixed Si/SiC 3-level converter, using the methodology developed in Section II to predict the thermal loading and number of dies per solution. With the optimal number of dies calculated per topology, the impact of the 3-level topology on the reduction of parallel SiC MOSFET dies is quantified against that of the 2-level converter in terms of savings in die costs.

A. Reduction of Parallel Dies with Switched Neutral

After iterating towards an optimal number of parallel SiC dies per topology, i.e. by the flow described in Figure 4, and assuming a coolant temperature of 60°C, i.e. as per [16], the thermal distribution of each topology is calculated assuming a maximum junction temperature of 125°C.

The thermal distribution of the 3-level converter with 4 parallel SiC dies is illustrated in Figure 9 – given inverter mode operation at 70kW, 30° power factor angle with a switching frequency of 20 kHz. Under the same conditions, Figure 10 illustrates the 3-level converter with 4 parallel SiC dies under rectifier operation. In Figure 11, with the 2-level all-SiC converter, the same temperature rise is produced (inverter and rectifier mode are nearly equal in this case) with 5 parallel SiC dies. Therefore, the switched neutral of the 'T-type' 3-level converter alleviates the thermal constraints on the SiC MOSFET devices, allowing a reduction in the number of higher cost SiC dies. This result is due to the 3-level mixed Si/SiC converter having the same thermal loading per SiC die with 4 dies in total, as the 2-level all SiC converter with 5 dies in total (per equivalent device). In Figure 10 under dynamic breaking or rectification mode, the Si-based switched neutral is the primary limitation as the SiC MOSFET components are not stressed in comparison to the 2-level SiC converter. However, as the thermal constraints at the loading conditions are met, the 3-level converter uses a single IGBT die per equivalent device.

B. Loss Breakdown at Optimal Number of Parallel Dies

Using the methodology described in Section II, the 3-level mixed SiC/Si converter requires 4 parallel SiC MOSFETs for operation, and the all-SiC converter requires 5 parallel SiC MOSFETS for driving a bi-directional 70kW load at 20 kHz. Under inverter operation, Figure 12 illustrates that the majority of the losses are dominated by conduction losses in the SiC MOSFET components of each topology. Note here that the 'MOS SynR' component refers the SiC MOSFET operating in the third quadrant. Likewise, according to Figure 13, which illustrates the two topologies under the same operating conditions but under rectification mode, the conduction loss also forms the majority of the overall losses.

While it would appear that the 2-level converter has reduced conduction losses within the SiC MOSFETs, it should be noted that Figure 12 and 13 are derived from comparing different number of parallel SiC dies between the two topologies. Furthermore, it is expected that the overall conduction losses are higher for 3-level converters – due to the number of devices connected in series [2]. Therefore, in terms of conduction losses, the results of Figures 12 and 13 are not unexpected as the switched neutral of the 3-level converter only acts to alleviate stress of the reverse current path of the SiC MOSFETs in this case (note the lack of 'MOS SynR' conduction losses under inverter operation).

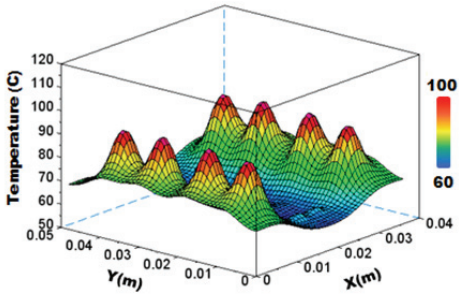

Figure 9. Single phase leg of the 3-level mixed Si/SiC converter on a 36mm by 48mm AlN substrate with a coolant temperature of 60°C. Inverter P_{out} = 70 kW and f_c = 20kHz.

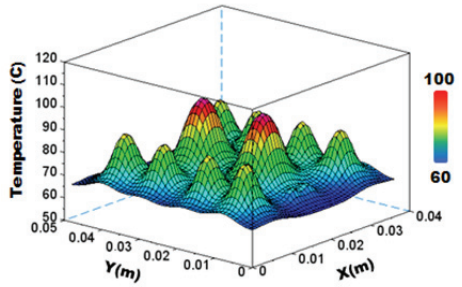

Figure 10. Single phase leg of the 3-level mixed Si/SiC converter on a 36mm by 48mm AlN substrate with a coolant temperature of 60°C. Rectifier P_{out} = 70 kW and f_c = 20kHz.

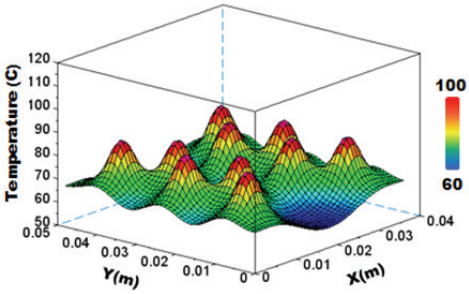

Figure 11. Single phase leg of the 2-level all SiC converter on a 36mmx48mm AlN substrate with a coolant temperature of 60°C. Inverter/Rectifier P_{out} = 70 kW and f_c = 20kHz.

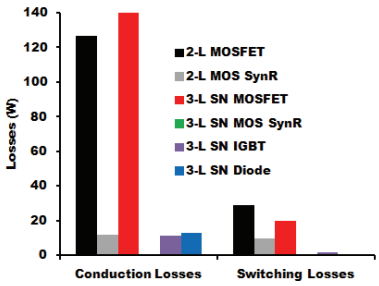

Figure 12. Breakdown of switching and conduction losses per component for the 2-level all SiC Converter and the 3-level SiC/Si switched neutral (SN) converter. Inverter P_{out} = 70 kW and f_c = 20kHz

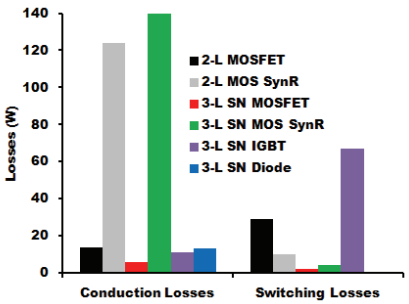

Figure 13. Breakdown of switching and conduction losses per component for the 2-level all SiC Converter and the 3-level SiC/Si switched neutral converter. Rectifier P_{out} = 70 kW and f_c = 20kHz

However, as reported in other works, i.e. [2], the switched neutral of the 3-level topology redistributes the switching stress from the SiC MOSFET dies to the IGBT dies – thereby illustrating the main contributing factor in the ability to allow the reduction of the number of parallel SiC MOSFET dies. Finally, under examination of Figures 12, it is reasonable to conclude that the switched neutral of the 3-level converter can be favorable with higher switching frequencies, but this falls out of the application domain considered in this paper.

C. Matched Phase Current Ripple

Due to the 3-level stepped voltage waveform, the phase current ripple of the electric machine is lowered by a factor of two. Therefore, while it is clear from Section III.B that the conduction losses are dominant in the application considered for this paper, the switching frequency of the 3-level mixed Si/SiC converter can be lowered to half or increased by a factor of two in the 2-level SiC converter to match the phase current ripple between the two topologies. For the sake of computational simplicity, the switching frequency of the 3-level converter is reduced by a factor of 2.

Figure 14 and 15 illustrates the 3-level mixed Si/SiC topology with a 10 kHz switching frequency, on the same substrate area and operating conditions as in Figures 9 and 10. By the reduced switching losses, but increased condition losses, the number of parallel SiC MOSFET dies is able to be reduced to 3 – with a maximum temperature of just under 125°C. Therefore, assuming the identical phase current ripple within the electric machine, the application of the 3-level converter is further able to reduce the number of higher cost SiC dies necessary for the power module construction – albeit with decreased conversion efficiency.

DISCUSSION

In this section, the implications on die cost and overall costs for the mixed Si/SiC 3-level converter is discussed against that of the 2-level SiC converter.

The ability of the Si-based IGBT switched neutral to reduce the losses in the SiC MOSFETs of the 3-level converter is largely shown to be related to switching loss redistribution. Hence, given the application requirements, the number of SiC MOSFET dies is able to be reduced by 1 per device combination – or 6 dies in total. In Figure 16, it can be seen that with the 4 dies, the 3-level mixed Si/SiC is able to achieve

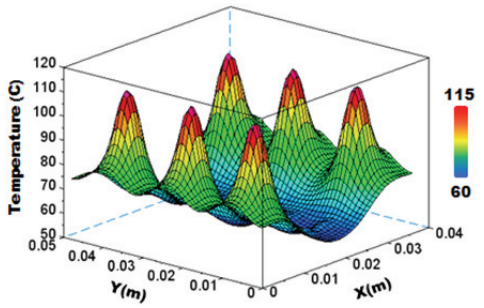

Figure 14. Single phase leg of the 3-level mixed Si/SiC converter on a 36mmx48mm AlN substrate with a coolant temperature of 60°C. Inverter P_{out} = 70 kW and f_c = 10kHz.

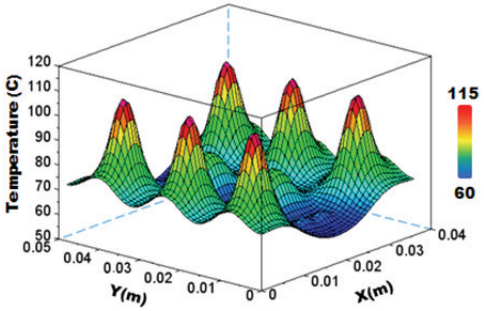

Figure 15. Single phase leg of the 3-level mixed Si/SiC converter on a 36mmx48mm AlN substrate with a coolant temperature of 60°C. Rectifier P_{out} = 70 kW and f_c = 10kHz.

the same efficiency as the 2-level SiC converter with 5 SiC MOSFET dies per device. While the rectification mode causes a slight decrease in efficiency (0.6%), it should be noted this condition cost be acceptable given the driving cycle requirements. Therefore, assuming an optimal target for efficiency versus die costs, the 3-level mixed Si/SiC uses 4 SiC MOSFET dies, while the all-SiC 2-level converter uses 5 SiC MOSFET dies per device.

Therefore, in terms of die cost, the Si/SiC 3-level converter can be compared against the SiC 2-level converter. As manufacturing costs decrease over time, the die costs between the two converters is represented in Figure 17 using a ratio between SiC dies and Si dies – where a relative cost of 1.0 between SiC dies and Si IGBT dies represents equal costs between them (with the die areas used in Table 1). While the number of SiC dies is decreased by 1 per equivalent device, the addition of the switched Si-based IGBT neutral increases the initial cost of the 3-level converter. Thus, only after a cost ratio of beyond 2.0 does the 3-level Si/SiC converter begin to be competitive in terms of die cost. It should be stressed here that with increased device switching frequency (i.e. beyond the application requirements given in this paper), the 3-level Si/SiC converter would be more cost effective.

While the use of the 3-level converter is advantageous for machine efficiency and lower EMI production [2, 3], considering the power module construction, as shown in Figure 1, and the application requirements, the 2-level all SiC has three appealing characteristics. In particular, the 2-level converter has half the number of gate drivers, and lower control requirements. The latter aspect refers to the use of a split-capacitor connection on the 3-level converter, and therefore,

some degree of capacitor balancing is necessary for robust operation. Most importantly though, due to the presence of the MOSFET body diode and reverse channel conduction, the 2-level module can be constructed from dies with identical die height – greatly simplifying the construction effort of a module with double-sided cooling [17].

Thus, since the conduction losses dominate due to the specifications of the application, the die cost savings provided by the 3-level converter (~12% at a relative cost of 4.0) is not substantial enough compared to the increased packaging, control and gate driver costs. Despite this immediate result, the 3-level topology remains an interesting approach if the switching frequency was significantly higher – allowing a significant reduction of the number of parallel SiC MOSFETs - or if line filters were required in the application.

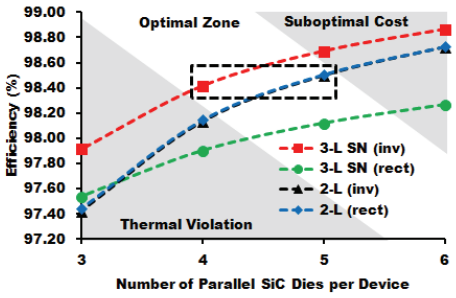

Figure 16. Comparison of conversion efficiency against the number of parallel SiC dies per device under inverter and rectification mode for the 3-level mixed Si/SiC converter and the 2-level SiC converter. Inverter/Rectifier P_{out} = 70 kW and f_c = 20kHz.

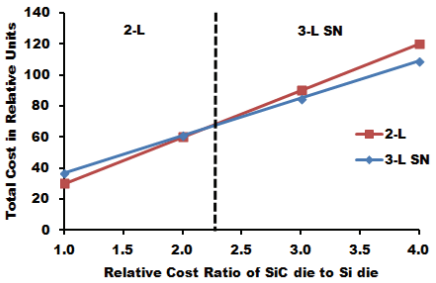

Figure 17. Relative cost of the SiC dies to the IGBT die (1.0 per-unit) and the impact on the overall die cost of the 2-L converter (5 dies) and the 3-L SN converter (4 dies)

CONCLUSION

This paper investigated the possibility of using a low cost Si based switched neutral to reduce the number of SiC dies was investigated for use in a high performance power module with double sided cooling for high speed drive applications. A methodology was therefore developed to compare the addition of the IGBT Si-based switched neutral against a 2-level SiC converter in terms of number of parallel SiC MOSFET dies utilized using a 20 kHz switching frequency, and driving a high speed machine capable of 70 kW operation. It is found that two topologies can achieve similar conversion efficiency, with the 3-level converter requiring one less high cost SiC MOSFET die per equivalent device. While the 3-level mixed Si/SiC converter topology is appealing as it can reduce the number of required SiC MOSFET dies for a given power level, in the considered application conditions, the die cost is not enough to overcome the additional complexity in terms of gate drivers, split-capacitor control and packaging design.

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