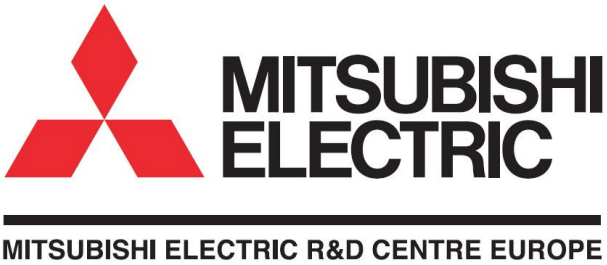

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Improving the die utilization and lifetime in a multi-die SiC power module by means of integrated per-die gate buffers

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Improving the Die Utilization and Lifetime in a Multi-die SiC Power Module by means of Integrated Per-die Gate Buffers

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***Abstract*—the full utilization of the active devices within a SiC power module can be limited by the common stray inductive path imposed by the substrate layout. In this paper, the prospect of integrating individual gate buffers per power die is explored for lowering the total losses of a power module, while maintaining a good thermal distribution across the set of dies. Each die within the power module has an increased utilization due not only having lowered losses, but due to the similar source inductive path for die, similar thermal loading. Using a 50kVA, 1.2kV, 8-die prototype power module, the overall switching losses using per-die buffers is found to be reduced by a factor of 25%, while significantly improving the thermal distribution from die to die.**

Keywords—multi-die SiC power module, integrated gate driver, hotspot temperature reduction.

I. INTRODUCTION

As the switching speeds of modern SiC power devices increase, the impact of the layout and the properties of the individual semiconductor chips limit the full potential of power module – especially with a high number of dies. Specifically, as the number of parallel dies increase, the physical path from the gate and source of the gate driver to the individual gate pads must also increase, resulting in an unbalance in the thermal loading of each die - thereby making a de-rating factor mandatory for safe operation [1-3]. While the layout of the substrate can mitigate the unbalance to some degree, increasing the total gate resistance can also decrease this balance to some extent, otherwise more advanced gate driving techniques might be necessary [4]. Finally, other effects such as the gate threshold voltage variations only add to thermal asymmetry in the power module, requiring a current rating of the power module to be lower in order to maintain a given maximum junction temperature limit for all dies [5].

In a standard multichip power module, a single gate driver is used to control all dies in parallel, as shown in Fig. 1 (b). In this paper, the prospect of integrating per-die gate buffers, as shown in Fig. 1 (a), is investigated to reduce the total losses and improve the thermal profile within the power module. The effect of having per-die buffers minimizes the gate loop inductance, and the effect of an increasingly unequal source inductance across several dies is minimized – enabling fast switching speeds and a more homogeneous distribution of the die temperatures. Therefore, this paper aims to show that standard power modules with SiC devices can be better utilized by integrating a gate buffer for each die within the gate driver.

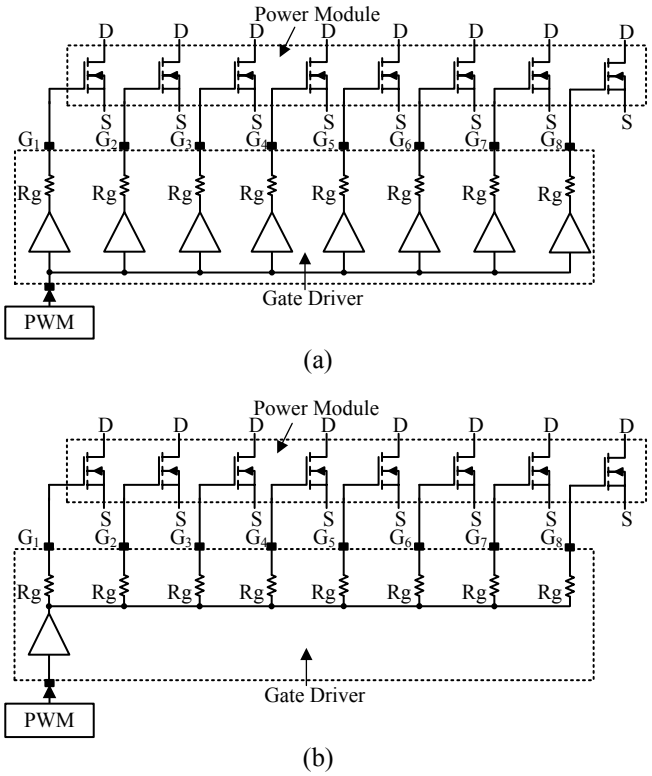
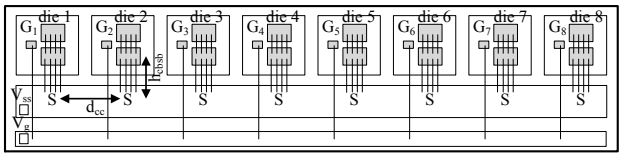


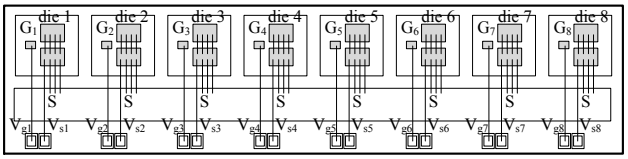
Fig. 1. Eight die power module with a single gate driver and (a) integrated per-die buffers and (b) single stage buffer

II. INTEGRATED GATE BUFFERS

In this section, the effect of an increasing number of parallel dies is related to an increasingly unequal parasitic source inductance for each die. The differences obtained with integrated per-die gate buffers are highlighted, and the impact of the source inductance and gate resistance is related to the switching loss in each die. Finally, the consequences in terms of the unbalanced loss distribution across a hypothetical 8 die power module are discussed in terms of an increasing gate



(a)



(b)

Fig. 2. Substrate layout of two approaches: (a) single gate buffer employment and (b) per-die gate buffer employment. The distance between dies is given as d_{cc} and the length of the wire bond is given as h_{cbsb}

resistance and threshold voltage differences. Hence, it is shown that per-die buffers can be an alternative method to complex packaging techniques for improving the utilization of the power module and the devices integrated within.

A. Source Inductance Considerations with Parallel Dies

Typically, within a current power module, the source potential of each die is connected along a low-inductance bus-bar, as shown in Fig. 2 (a), terminating at the point V_{ss}. Assuming that the spacing between the dies, $d_{cc} = 1.5\ cm$, the bus-bar has an incremental inductance $L_{bsb} \cong 1.5\ nH/cm$ and that the wire bonded connection is equivalent to 10 nH, the incremental source inductance from V_{ss} to die 'n' follows (1):

$$\Delta L_s = L_{bond} + n \cdot L_{bsb} \cdot d_{cc} \dots (1)$$

Therefore, with 8 dies in a power module, the source inductance path differs by up to 18 nH, between die 1 and die 8, with a total source inductance of 29.5 nH in the latter case. While alternative layout methods exist to reduce the distance of each source pad connection to the driving point of the buffer, it is clear that having per-die connections will enable a minimization of each source inductance loop for driving the parallel dies.

B. Switching Losses as a Function of Source Inductance

Owing to the reduced gate voltage during the drain current evolution, the switching losses of each die can be negatively impacted by the magnitude of the source inductance, especially under high di_D/di conditions [6]. Specifically, for the purposes of illustrating the impact of reducing the source inductance mismatch from die to die, the drain current in a MOSFET device can be linked to the difference in the gate voltage, $v_{gs}(t)$, and threshold voltage, V_T, and the transconductance, g_{fs} via (2). During the drain current evolution during either device turn on or turn off, the switching loss during this period can be approximated as being proportional to the integral to a function of the gate voltage via (4) from (3), especially if $V_{dc} \gg (L_s + L_d)di_D/d_t$.

$$i_d(t) = g_{fs} \cdot \left(v_{gs}(t) - V_T\right) \dots (2)$$

$$E_{loss} = \int i_{ds}(t) \cdot v_{ds}(t) dt \dots (3)$$

$$\therefore E_{loss} \propto \int f\left(v_{gs}(t)\right) dt \dots (4)$$

Therefore, before the miller plateau region, the gate voltage can be defined during this period according to (5), assuming an under-damped system, with R_g signifying the gate resistance, C_{iss} - the input capacitance of the device, and V_{gh} - the gate voltage, respectively [6]. Note that only the turn-on transition is considered due to brevity, but the process is similar for the turn-off transition.

$$v_{gs}(t) = V_{gh} - \left(V_{gh} - V_T\right) \cdot e^{-\frac{t}{R_g \cdot C_{iss} + L_s \cdot g_{fs}}} \dots (5)$$

Hence, it can be shown then that the switching losses are approximately related to the source inductance and gate resistance via (6). Given a source inductance between dies with otherwise similar parameters, the relative increase in switching losses incurred before the miller plateau region can therefore be determined.

$$E_{loss} \propto L_s \cdot e^{-\frac{t}{R_g \cdot C_{iss} + L_s \cdot g_{fs}}} \dots (6)$$

C. Unequal Loss Distribution with Parallel Connected Dies

In order to visualize the effect of the incremental source inductance for each parallel die, according to (1), and (6), the parasitic of the power module with a single buffer can be modeled accordingly as in Fig. 3. Considering the bus bar length for each die as previously given in Fig. 2 (a), and a fixed gate resistance driving a hypothetical 8 die power module, the relative switching loss increase before the miller plateau region can be illustrated, as shown in Fig. 4. Note that in Fig. 4, the switching losses are illustrated relative to die 1, i.e. the die closest to V_{ss}.

With minimal gate resistance, the spread of the relative switching loss is nearly 2.5 that of die 1 – resulting in a significant asymmetry in the power loss profile for a switching loss constrained application, i.e. most practical applications. However, while adding additional gate resistance can mitigate the switching unbalance to some extent, i.e. reducing the relative switching loss in the worst case from 2.5 to 1.6 the large gate resistance required implies a significant increase in total switching losses.

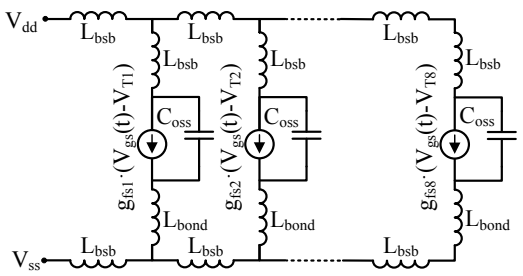


Fig. 3. Equivalent parasitic representation of each parallel dies in Fig. 2 during active commutation with C_{oss} representing each device output capacitance

Therefore, given a large power module, the gate resistance must provide a trade-off between the peak temperature of the hottest die, and the total power module losses. Alternatively, a more common approach is to de-rate power module for a given load current to ensure safe operation under the maximum junction temperature of each die for a nominal gate resistance value. Clearly, by keeping the source inductance path to each die virtually identical, the losses in the power module would then be more evenly distributed, while allowing for lower gate resistances to be employed, and thereby minimizing the overall power module losses.

Another point of consideration is the impact of a distribution in threshold voltages within the power module on the relative switching losses across the dies. While threshold voltages can be screened and the differences therefore minimized, an increasing source inductance has nevertheless an incrementally negative impact with an increasing variation in threshold voltages across the parallel dies. The impact of the variance in threshold voltage can be visualized in Fig 5, all relative to Die 1 with threshold voltage of 3.5V. Clearly, with an increasing disparity in threshold voltages, the impact of the increasing source inductance has a large impact on the switching losses.

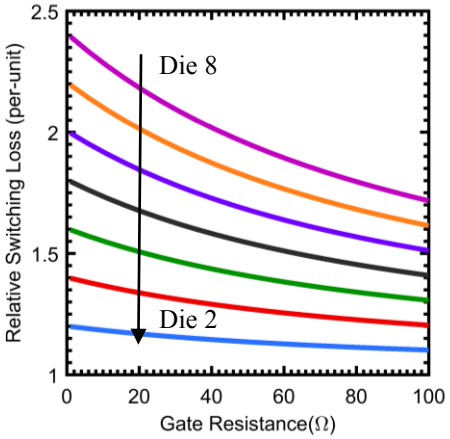


Fig. 4. Relative switching losses (during the current commutation period) of each die in a hypothetical 8-die power module with increasing gate resistance

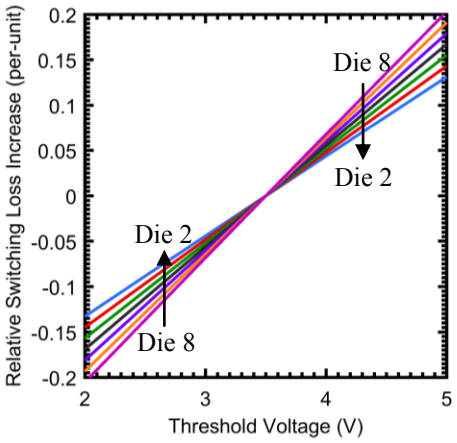


Fig. 5. Relative switching losses (during the current commutation period) of each die in a hypothetical 8-die power module with increasing variations in the threshold voltage (normalized to 3.5V)

III. Experimental Results

Conceptually, integrating per-die gate buffers within the power module reduces the source inductance path asymmetry from die to die, and reduces the overall inductive gate loop to achieve minimal losses. Therefore, this section is dedicated to the experimental validation of a discrete version of the power module investigated with the aim to illustrate the potential of the per-die buffer approach to improve die utilization and therefore the lifetime of the power module.

A. Experimental Design

While the per-die buffer integration is aimed at a multi-chip power module, prototype was constructed using 8 parallel 1.2 kV / 20 A discrete SiC MOSFET devices, as shown in Fig. 6. Further, a heat-sink was designed such that the fan was closest to die 1, and furthest from die 8 – causing a significant difference in the thermal profile. Another power module was designed with the same devices and layout concept, but with a single buffer for all the dies – herein called the reference power module. Thus, using discrete components, the two substrate layouts of Figs. 2 (a) and (b) have been replicated for experimental testing.

In order to identically load all devices, the power modules are connected in a full bridge configuration using only a load inductance of 1.5mH. Hence, under these similar conditions, the two power module implementations can be better understood and compared.

Firstly, owing to the differences in the gate driver loop inductance, the reference power module required a larger gate resistance to achieve the same slightly under-damped response as the per-die driven power module. Hence, with the per-die driven power module, a smaller gate resistance resulted in the same peak drain current between the two implementations, as shown in Fig. 7. With this method, the per-die driven power module was operated with 12 Ω of gate resistance, compared to the reference power module with 20 Ω.

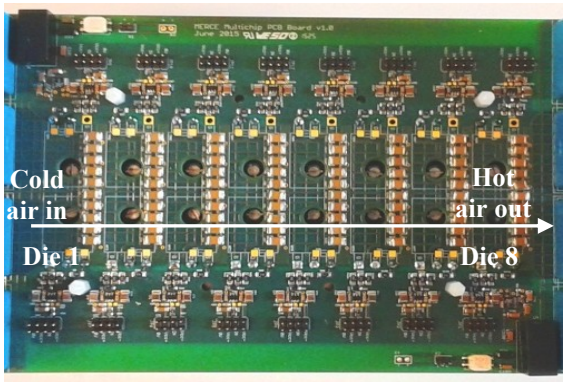


Fig. 6. Experimental prototype power module with per-die buffers for a half-bridge configuration. The air flow from left to right and all results are obtained with 600V dc bus, 50A load current and a 200 kHz switching frequency

B. Improved Die Utilization and Lifetime

Employing the two 8-die power modules under the designed operating conditions, the per-die driven power module achieves lower losses for the same current. Specifically, as illustrated in Fig. 8, the turn-on switching losses are reduced by approximately 25%, when measuring the

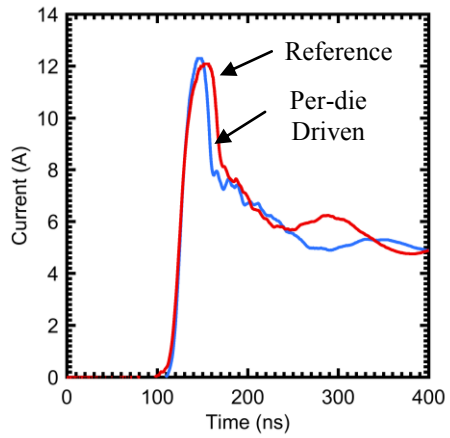


Fig. 7. Drain current evolution during the turn-on commutation period of the hottest die in the reference and per-die gate buffer configurations (experimental)

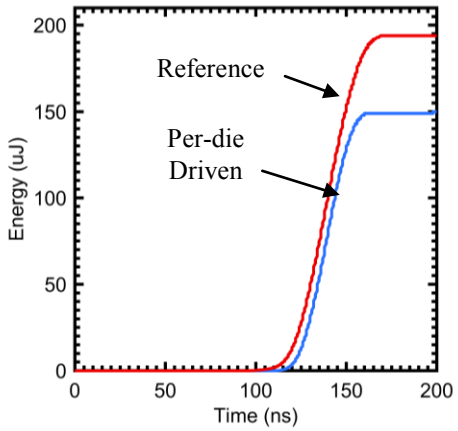


Fig. 8. Turn-on switching energy of the reference and per-die gate buffer configuration (experimental)

hottest die of each power module. Note that the oscillations in the switching energy have been eliminated for graphical clarity. Therefore, the per-die driven power module can achieve significantly lower losses, allowing for a higher current rating for an associated power envelope of the package.

The reduction in losses obviously translates to a lower peak junction temperature across the set of parallel dies. Using a high resolution thermal camera, the average surface temperature over each discrete die was measured in both power modules. In the per-die driven power module, the peak junction temperature was measured at $71°C$, whereas the reference module had a peak temperature of around $83°C$, as shown in Fig. 9.

Clearly, while the reduction of the peak junction temperature indicates the ability to process more power for a given temperature limit, a significant result of Fig. 8 is related to the reduction in the temperature dispersion of each die relative to the mean temperature of the power module. In the reference module, relative to the mean temperature, the hottest and coldest dies are further apart ($+7.5°C$ and $-6.5°C$) compared to the per-die driven module ($+6°C$ and $-5°C$) - indicating a better thermal spread in addition to reducing the total losses in the power module. Consequently, as there is a significantly larger thermal margin ($12°C$) with smaller thermal spread, the die utilization has effectively been increased, allowing an increase in the power density for a given package.

Alternatively, the reliability of the power module can also be considered, assuming that the module is cooled to ambient temperatures on a regular basis. Using the Coffin-Mason law cycle fatigue relationship, as per (7) with n = 4.31, the lifetime has increased by a factor of 4.3 in the per-die driven power module compared to the reference power module [7].

$$\frac{N_{f,1}}{N_{f,2}} \propto \left(\frac{\Delta T_{j,2}}{\Delta T_{i,1}}\right)^n \quad \ldots (7)$$

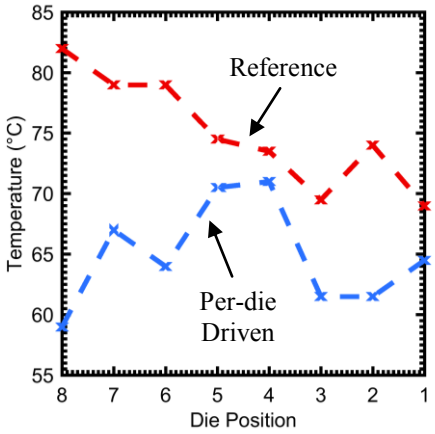


Fig. 9. Peak die junction temperature across the reference and per-die buffer configurations (experimental)

IV. Conclusion

In this paper, the gains from integrating per-die buffers in a multi-die power module were explored. It was illustrated that the inherent inequalities, in terms of source inductance paths and die parameters, contribute to an unequal thermal profile in the power module. Introducing individual buffers to each die mitigates these inequalities, with a subsequent reduction in losses and improved die utilization.

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