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A Highly Efficient 2kW 3-Level Full-MOSFET Inverter

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Keywords

«MOSFET Inverter», «Multi-level», «Flying capacitor», «Soft-switching».

Abstract

This paper investigates an improved 3-level flying capacitor inverter topology allowing a drastic reduction of reverse recovery related losses. It benefits from the latest superjunction (SJ) MOSFET devices. The presented 2kW inverter was designed for Japanese PV market (200Vrms). It allows non unitary power factor operations with peak and European efficiency of 98.0% and 97.6% respectively. Thanks to SJ MOSFET implementation, it outperforms state-of-art configuration using IGBTs and SiC diodes in terms of efficiency.

Introduction

Silicon Superjunction (SJ) MOSFETs [1] provide excellent static and dynamic performances at voltage range of 600/650V. However, the parasitic body-diode demonstrates poor switching behaviour (high reverse recovery charge Q_{RR} and slow commutation speed dV/dt and dI/dt). Design parameters (e.g. doping concentration and base thickness) that improve the MOSFET performances degrade the performances of the diode [1, 3] and both components cannot be optimized. As a consequence, in many AC applications, the body diodes are unusable and IGBTs are usually preferred to MOSFETs.

Additional diodes and/or saturable inductors were introduced in [3] to alleviate the issue with body diodes by forcing the reverse current into an external diode. A H6-type one-level MOSFET inverter without power factor control was presented in [4]. The large turn-on losses, ruggedness and EMI problems induced by the body-diode are alleviated by making the diodes inactive, i.e. alternative current paths are created through 2 additional MOSFETs and diodes.

In this paper, an improved topology allowing the full use of SJ MOSFETs in a highly-efficient 2kW multilevel single-phase inverter with power factor control is presented. The topology makes use of soft-switching snubbers to tackle the reverse recovery related issues while reducing the dynamic losses. First, the topology with the lossless turn-on and turn-off snubber is described. Then, a loss model is presented, based on experimental loss measurements in both hard and soft switching conditions. The performances of the inverter are compared with different semiconductor devices (MOSFETs and IGBTs) with and without the snubber. Then, the paper gives some experimental waveforms and efficiency curves of the inverter to validate the theoretical analysis and the loss model. Finally, a cost analysis is performed to complete the evaluation of the topology with various semiconductor devices.

Description and analysis of the inverter topology

Soft-switching 3-level flying capacitor topology

The specifications for the case study are given in Table I. The 3-level flying capacitor topology with unbalanced voltage levels for outer (600/650V) and inner (250/300V) cells was selected as the best architecture that fits the design requirements [5], not only for efficiency but also to be compliant with the PV leakage current related issues. In the basic configuration, it is unfortunately impossible to use

SJ devices due to the fact that the corresponding body diode has poor switching performances. To make it possible, the following section presents topology improvements (Fig. 1) that alleviates this issue and allows the use of MOSFETs for all active switches.

Table. 1: Converter specifications	
Ambient temperature	-15~40°C
Input input voltage	250 - 420V
Grid voltage	160 - 240V
Grid, frequency	50/60Hz
Rated output power	2.0 kW
Output power factor	$\cos(\phi) \ge 0.85$ (Ind-Cap)
Harmonic distortion	Below 5% (<3% for each harmonic)



Fig. 1: Soft-switching 3-level flying capacitor topology (single leg)

Topology improvements

The control of the body diode switching is managed differently for the "low voltage" inner cell and the "high voltage" outer cell.

The inner switching cell (Fig. 1) still operates under hard switching conditions. This is not too detrimental to the switching losses because it uses fast 250V devices. A dual Buck derived topology operating with Bipolar PWM strategy was selected to alleviate recovery issues. Even if the Body diode is involved during operation, the dI/dt is controlled via an additional inductor which helps reduce the recovery charge while the switching transitions use ZVS techniques with the output capacitance C_{OSS} . In the outer cell, a loss-less turn-on and turn-off snubber was implemented (Fig. 1). The inductor L_{SN} controls the dynamics of the current and significantly reduces the turn-on losses (ZCS). Note that the snubber inductor L_{SN} is located between the upper switch and the top switch of the inner cell to enable bootstrap power supplies for the flying capacitor cell, but other locations are possible. The capacitors C_{SN1} and C_{SN2} are used to perform ZVS during turn-off transitions. The regenerative transitions involve the flying capacitor C_{FC} which acts as an energy buffer as further described.

Theoretical analysis of the loss-less snubber

Figures 2 and 3 describe the basic mechanisms of the snubber during the switching transitions of devices M_1 and M_2 . According to the duty cycle D, the flying capacitor location is different in the main switching cell. For D<0.5, the flying capacitor is located between the bottom switch and the connection point to the load. For D>0.5, the flying capacitor is in between the snubber inductor L_{SN} and the connection point. For the sake of clarity, the inner cell is replaced by a voltage source V_{FC} arbitrarily operating with D<0.5.

Turn-on transitions of M₁/ Turn-off transitions of M₂ (Fig. 2)

Stage 1: Linear charge/discharge of the snubber capacitors $C_{SN1\&2}$

 M_2 is turned off. Assuming that M_1 is not simultaneously controlled, the current flows through the snubber capacitors C_{SN1} and C_{SN2} , defining the ZVS transitions. The voltage rise and fall times linearly depend on the current value as well as the capacitors value. This stage stops as soon as the voltage across the device M_1 reaches zero ($V_{Csn1}=V_{FC}$).

Stage 2: Resonant Mode

A resonance occurs between the snubber elements L_{SN} and $C_{SN1\&2}$. The output current is flowing across M_1 except for the resonant current that flows in the paths depicted in blue in the Fig. 2 This stage continues until the diode D_{SN1} gets conductive, i.e. for $V_{Csn1}=0$. Note that the resonance may stop earlier if the snubber inductor is fully discharged before half the resonant period. Given the complexity of describing all stages with partial ZVS, this case will not be detailed here. Operate under Zero-Voltage transitions requires the electromagnetic energy W_{mag} to fulfil the following condition:

$$W_{mag} \ge W_{cap} \iff \frac{1}{2} \cdot L_{SN} \cdot I^2 \ge \frac{1}{2} \cdot L_{SN} \cdot I_{ZVS}^2 = \frac{1}{2} \cdot \left(C_{SN1} + C_{SN2}\right) \cdot V_{FC}^2 \tag{1}$$

When D_{SN1} is conductive, M_2 is exposed to the DC bus voltage V_{DC} .

Stage 3: Final demagnetization of L_{SN} via the flying capacitor

Both diodes D_{SN1} and D_{SN2} are conductive. The voltage V_{FC} is applied across the snubber inductor which finishes discharging linearly through the flying capacitor.

Stage 4: Parasitic resonance involving C_{OSS} and L_{SN}

When the demagnetization of L_{SN} is achieved, the diode D_{SN2} gets reverse blocked. The parasitic capacitance C_{OSS} of M_2 along with the stray capacitance, in particular the one from the flying capacitor cell, resonates with L_{SN} until the voltage across M_2 reaches its steady-state value V_{DC} - V_{FC} .





Turn-off transitions of M₁/ Turn-on transitions of M₂ (Fig. 3)

Stage 1: Linear magnetization of the snubber inductor L_{SN}

Due to the presence of L_{SN} , it would be possible to overlap the control patterns of M_1 and M_2 . Unfortunately, this mode slightly increases the constraints on the snubber diodes if the duration is not adequate. This remark is even more relevant for light loads. With the motivation to optimally design the snubber, M_1 is first turned off but keep in mind that overlapping is still possible without any risk of failures. With the selected assumptions (I>0), the current continues to flow through its Body diode. Then M_2 is turned on. The voltage across M_2 drops to zero without any previous Miller phase and the current in L_{SN} and in the conductive channel of M_2 rises linearly. This stage lasts until the current in the body diode of M_1 cancels. Consequently M_1 gets reverse-blocked assuming that the contribution of the recovery current remains small.

Stage 2 : Resonant Mode

The snubber elements L_{SN} and $C_{SN1\&2}$ start resonating to discharge C_{SN2} and charge C_{SN1} . This stage continues until the complete charge of C_{SN1} , i.e. for $V_{Csn2}=0$. In order to achieve the complete discharge of C_{SN2} and full ZVS on M_2 during its turn-off transitions, the voltage across the flying capacitor must be wisely chosen. Derived from the analytical calculation, the condition to fulfil is (2).

$$V_{DC} \ge 2 \cdot V_{FC} \tag{2}$$

The peak current through L_{SN} , which is useful to define the saturation level, is given by (3) :

$$I_{pk} = I_{max} + (V_{DC} - V_{FC}) \cdot \sqrt{\frac{C_{SN1} + C_{SN2}}{L_{SN}}}$$
(3)

When D_{SN2} gets conductive, M_1 is exposed to the DC bus voltage V_{DC} .

Stage 3 : *Final demagnetization of* L_{SN} *via the flying capacitor*

Both diodes D_{SN1} and D_{SN2} are conductive. The voltage V_{FC} is applied across the snubber inductor which linearly demagnetizes down to the load current I.

Stage 4 : Parasitic resonance involving C_{OSS} and L_{SN}

When the demagnetization of L_{SN} is complete, D_{SN2} gets blocked. Likewise the other switching transitions, M_1 reaches its steady-state value V_{DC} - V_{FC} after a resonance involving the MOSFET's output capacitance and the stray capacitance within the PCB.



Fig. 3 : Principal waveforms during the turn-off transitions of M₁
Currents : M₁ (black), M₂ (dashed black), L_{SN} (grey)
Voltages : M₁ (black), capacitors C_{SN1} (dashed), C_{SN2} (grey)

Efficiency comparison of various combinations of active devices

In this section, three different solutions are compared to equip the main switching cell: a MOSFET (and its body diode), a fast IGBT using a hyper-fast Silicon diode (respectively FGB40N60SM and RUR1S1560S from Fairchild) and a combination of a fast IGBT with a Silicon Carbide diode (IDD12SG60C). The switching losses are evaluated experimentally for the three solutions, the loss models are built, and the loss breakdowns are presented. For the inner cell, experimental measurements of the recovery charge, voltage and current dynamics (dV/dt and dI/dt) were carried out to select the gate resistances with the motivation being to optimize the switching losses without affecting the reliability.

Experimental switching loss estimation with a double pulse tester

As mentioned before, MOSFETs are only considered if soft switching is possible, mainly to cope with the poor dynamic performance of its body diode. If the topology operates with IGBTs, several implementations are still possible. Since our goal is to reach a high efficiency level, a combination with a conventional diode operating under Hard Switching (HS) conditions was not considered. Then, our intention was to demonstrate the relevancy of using soft-switching with IGBTs that suffer from stored charge even in the case of ZVS [6]. Also, a comparison between a soft switched (ZCS) Silicon diode and a hard switched SiC diode was carried out. The switching losses in the devices were estimated with a double-pulse tester (DPT), as depicted in the Fig. 4. The switching transitions dictated by the proposed snubber were emulated with a RCD snubber to control the dV/dt during turn-off and a RLD snubber for the dI/dt during turn-on, see Fig. 4.



Fig.4 : Schematic (left) and picture (right) of the double pulse tester with ZVS/ZCS snubbers

Switching energies of a switching cell including an IGBT with a SiC diode

With the proposed snubber in the flying capacitor topology, the voltage to withstand by the devices in the inner cell requires 600V switches even if the flying capacitor voltage is around 200V. Two sets of measurements were performed to extract correlations laws. With a constant voltage of 200V, the switching losses were first measured for increasing values of currents from 5 to 30 Amps (Fig. 5). To complete the protocol, the voltage dependencies were investigated for a constant current value (30Amps) (Fig. 6). A least mean square fit was used to define the parameters of a polynomial correlation for both ON and OFF energies.

Turn-on energies of an IGBT and a fast Si Diode operating with Zero-Current switching (ZCS)

Under hard switching conditions, the dynamics of current depend on both the gate drive and the IGBT characteristics. During the turn-on transitions, the voltage across the switch is reduced due to a voltage drop across the stray inductance L_{σ} .dI/dt. With high enough stray inductance or very fast control (low Rg, high transconductance), V_{CE} (respectively V_{DS} for MOSFETs) can even be cancelled. Under these conditions, the turn-on losses are theoretically cancelled. One advantage of pseudo-ZCS is to significantly reduce recovery-related effects. Although the peak recovery still exists, its contribution to the switching losses can be neglected since the voltage across the controlled device is null. This mode clearly favours Silicon diodes which demonstrate much better static performances compared to SiC

diodes. Illustrative waveforms (from measurements) are given in Fig. 7 and 8 as comparative results of turn-on energies between hard-switched SiC and hyperfast diodes with ZCS.

The data shows that ZCS transitions outperform a switching cell involving a SiC diode even for small inductor values (reduction of at least a factor of 2 with 1 μ H). With a typical value of 1000A/ μ s (even higher for Superjunction devices), 200nH would be enough to achieve pseudo-ZCS. Since the inductor value also defines the peak overcurrent as well as the ZVS range, values from 4.7 μ H to 10 μ H were selected which means that E_{on} can reasonably be neglected.



Fig. 5: Switching energies for various I at 200V



Fig. 7: Comparative turn-on waveforms in a switching cell using an IGBT and a fast diode



Fig. 6: Switching energies for various V at 30A



Fig. 8: Ratio of turn-on energies with a SiC diode and a soft switched fast diode

Turn-off energies of an IGBT operating under Zero-Voltage switching (ZVS)

Under hard-switching conditions, a significant contribution to the turn-off losses stems from the IGBT tail current. Because both electrons and holes coexist in the drift layer, a recovered charge (depicted in yellow in Fig. 9) has to be extracted. Even with soft switching techniques, a few hundreds of ns are usually mandatory to get rid of this phenomenon due to the recombination process and the carrier's transit time. From a qualitative point of view, the "recovery" process is also sped-up by applying an electric field across the device (voltage) which reduces the carriers' transit time inside the drift layer, irrespective of recombination times. This is the reason why there is an optimal value to implement in case of capacitively assisted switching transitions [7][8]. For example, if C_{ext} is too high, the voltage slowly rises and the charge extraction is only weakly assisted.

For the selected IGBT (FGB40N60SM), a campaign of measurement was carried out for several values of external capacitors to define the best trade-off between loss reduction and design constraints of the snubber - a bigger capacitive energy directly increasing the overcurrent during resonances while reducing the ZVS range. From Fig. 10, it can also be highlighted that the ZVS contribution is nearly constant once the capacitor exceeds 10nF since an increase of 50% (from 2x4.7nF to 3x4.7nF) reduces the losses by less than 20%. Based on these results, it can also be concluded that loss reduction by ZVS beyond 50% cannot be realistically achieved with the IGBTs.



Fig. 9: Comparative turn-off waveforms of an IGBT with external capacitors



Model-based loss analysis of the inverter with MOSFETs

Conventional conduction formulas were used to complement the loss calculation for the active devices (diodes and MOSFETs). The junction temperature was assumed to be 125°C which corresponds to a pessimistic case from a thermal point of view, more especially with unipolar components.

Concerning the filtering inductors, an automatic design procedure was first implemented to see how sensitive the cost and the conversion efficiency were according to the current ripple or the switching frequency. To both simplify the filtering requirements and the losses calculation, an equivalent RMS voltage across the inductor was analytically derived according to the modulation depth R_m of the inverter. The inductor copper losses were estimated thanks to a modified Dowell approach targeting toroidal geometries [9][10]. The results were confirmed with FEA simulations with FEMM environment. Core losses were basically calculated with the Steinmetz coefficients from manufacturers' datasheets.

The snubber inductor L_{SN} acts as a pulse inductor and is exposed to a wide current spectrum. The high frequency behaviour is then critical to avoid excessive skin, proximity and iron losses. A campaign of measurement (Wayne-Kerr 6500) involving off-the-shelf products was carried out to select the most adequate snubber inductor L_{SN} . Based on estimated losses and thermal constraints, SER2900 from Coilcraft was finally selected.

The loss calculation also included the ESR of the flying capacitors, the DC-link and the associated damping circuits. Indeed, an additional RC network using SMD electrolytic capacitors (100 Ω / 47 μ F@250V) was implemented in the flying capacitor cell to absorb the low frequency harmonics (typically 100Hz) and avoid increasing needlessly the film capacitor bank.

Finally, to give a relevant overview of the converter performances, the PCB layout, the relays as well as the EMC common mode filter were taken into account.

Model-based loss comparison of the inverter with 3 implementations

Three different configurations were compared, loss breakdown shown in Fig. 11. The first two cases were analyzed with soft-switched MOSFET and IGBT (Infineon IPB65R045C7 and Fairchild FGB40N60SM respectively). When using a MOSFET, no freewheeling diode was considered. It is assumed that the body diode in conjunction with the MOSFET's intrinsic ability of operating in the third quadrant is suitable for inverter operations [11]. The soft-switched IGBT is equipped with an ultrafast diode (Fairchild RUR1S1560S). The third case involves an IGBT with a SiC diode operating under hard-switching conditions. The switching frequency is set to 30kHz, which finally appeared to be the best trade-off between efficiency and cost.



Fig.11: Loss distribution for different configurations of active devices with and without the snubber.

Results

Experimental waveforms

Figures 12 and 13 show experimental waveforms during turn-on and turn-off of the switch M_1 . The operating phases described previously can be recognized. With MOSFETs, a detailed analysis would show that the ZVS range is significantly altered by the highly non-linear capacitances of the MOSFET whereas the remaining Q_{rr} of its body diode increases the peak current in the snubber. Note that the latter point can be optimized by further reducing the dead-time between channels.





Fig.12 : Experimental waveforms during the turn-ON transitions of M_1 with MOSFETs



Experimental efficiency and models validity

The efficiency was measured experimentally and compared to the results of the modelling in Fig. 14-15. The calculated curve is within the accuracy bounds attributed to the power analyzer (Yokogawa WT3000). Its accuracy on the DC and AC sides are expressed by the equations:

Accuracy
$$DC = 0.05\% * reading + 0.1\% * range$$
 (4)

Accuracy
$$AC = 0.02\% * reading + 0.04\% * range$$

Ranges were selected to optimize the accuracy of the measurement. For the voltage and current levels considered, this leads to an absolute error of $\pm 0.3\%$ on the efficiency. When comparing the experimental efficiency curves with soft-switched MOSFETs and IGBTs in Fig. 14-15, the relative error between the two curves is close to zero because results are very reproducible and were performed in the same conditions. The converter with MOSFETs and IGBTs has a European efficiency of 97.6% and 97.3% respectively but with different efficiency curves. The MOSFET implementation has higher switching losses at low load because of much higher C_{OSS} values and poor diode performances that limit the ZVS range. However, the MOSFET has lower conduction losses at high current, which decreases the required cooling effort and potentially has an indirect beneficial influence on the product cost [12].

98.5





(5)





Comparison on cost/performance aspects with respect to hard switching topology Figure 16 shows a photograph of the board with the inverter legs. All the components being similar except for the snubber and the outer cell switches, the cost comparison for Multiple Order Quantity (MOQ) of 10k units can be easily performed for the 3 inverter combinations (Fig. 17).



Fig. 16: Photograph of the semiconductor parts and the snubber. 3/4: inner cell diodes, 2/5: inner cell MOSFETs, 1/6: outer cell 650 SJ MOSFETs



Fig. 17: Bill of material cost (10K MOQ) of an inverter leg for the 3 compared combinations

The snubber cost is estimated to be approximatively $3.5 \in$. The MOSFET inverter leg appears to be the most expensive, approximatively $14 \in$ more expensive than soft-switched IGBTs and $10 \in$ more expensive than hard-switched IGBTs equipped with SiC diodes. This is due to a higher cost of SJ devices. Implementing soft-switched IGBTs is the most cost-effective solution, because the additional cost of the snubber is less than the one of the SiC diodes.

To complete the comparison, additional advantages should be allocated to the soft-switched topology. First, in terms of EMI, the soft-switching converter generates fewer perturbations thanks to lower dI/dt and dV/dt. The EMI filter cost footprint is therefore potentially decreased. Finally, the robustness of soft-switched topologies is enhanced thanks to the presence of the inductance in series in the power leg that limits the current in case of leg short-circuit due to inaccurate dead-times.

Conclusion

This paper presents a high efficiency 2kW 3-level flying capacitor full-MOSFET inverter where bodydiode switching limitations are alleviated with a lossless snubber. The soft-switched inverter exhibits similar European efficiency when it is implemented with MOSFETs and IGBTs. However, the efficiency at nominal power is better with the MOSFETs, potentially allowing a reduced heat-sink volume and cost. On the other hand, the cost of super-junction devices penalizes the implementation of MOSFET. The presented topology clearly outperforms standard hard-switching implementations in terms of efficiency. Cost-wise, the best candidate is the soft-switched topology with IGBTs and silicon diodes. It has also the best efficiency/cost ratio. Finally, the presented soft-switched topology offers potentials for better EMI performances, and robustness.

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