IEEE Transactions on Power Electronics Vol. 31, No. 3, pp. 2200 – 2212, March 2016

DOI: 10.1109/TPEL.2015.2438036

A Soft-Switched Asymmetric Flying Capacitor Boost Converter with Synchronous Rectification

G. Lefevre
S. Mollov

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Guillaume Lefevre, *Member, IEEE*, and Stefan V. Mollov, *Member, IEEE*

***Abstract*—The multilevel flying-capacitor boost converter was analyzed for asymmetric voltage operation—this permits loss optimization that takes advantage of different voltage class MOSFETs. A cost-motivated design of a suitable zero-voltage zero-current switching snubber is then developed that permits a great reduction of the inductor size. With the proposed snubber, synchronous rectification operation is compared to that of diode boost, with a particular attention to the contribution of nonlinear MOSFET parasitics. Experimental results from a 2-kW/30-kHz prototype justify the effectiveness of this solution with a conversion efficiency around $99\% \pm 0.1\%$ for a wide load range.**

***Index Terms*—DC–DC power converters, efficiency, snubbers, soft-switching, zero-voltage zero-current switching (ZVZCS).**

I. Introduction

CONVERTERS increasingly target highest conversion efficiencies, not only at peak power but over a wide power range, while manufacturers intend to lower cost as much as possible while maintaining good performances [1]. In this context, the emerging wide bandgap (WBG) switches such as Silicon Carbide (SiC) or Gallium Nitride (GaN) appear as good candidates to reach these goals [2]–[4]. On the other hand, multilevel or interleaved topologies using Si devices are also competing alternatives. Soft-switching techniques appear as an interesting complement to reduce both losses and EMI emissions, e.g., [5]–[7]. The extra cost stemming from WBG devices or additional Si components allows nevertheless reducing the overall cost, in particular due to the magnetic components and possibly the heat management [8]. Fig. 1 summarizes how the cost, the weight, as well as the volume of a boost inductor evolve with respect to the effective energy W_{Eff} for two- and three-level topologies (identical design rules assumed). It is clear from Fig. 1 that the inductor cost is linearly dependent on the stored energy in the inductor.

Although it seems interesting to operate at extreme switching frequencies, it must be pointed out that this trend is capped by the EMI and thermal requirements. The decision of whether to use Si with multilevel topology or WBG is a fine balance between cost and volume associated with thermal management [8], [9]. Also, an increase of switching frequency implies fast commutations in hard-switched topologies, resulting in a bulky common mode (CM) filter. Finally, operating at medium frequencies with a multilevel topology is appealing since the inductor is drastically reduced and CM issues are alleviated by applying dedicated pulse width modulation (PWM) strategies [10]. In the example of Fig. 1, only a two-level boost operating at $8 \times 16 = 128$ kHz could compete with the design $n^{\circ}4$—three-level topology at 32 kHz. In addition, higher frequency designs will be more penalizing since skin-proximity effects and core losses become prevalent.

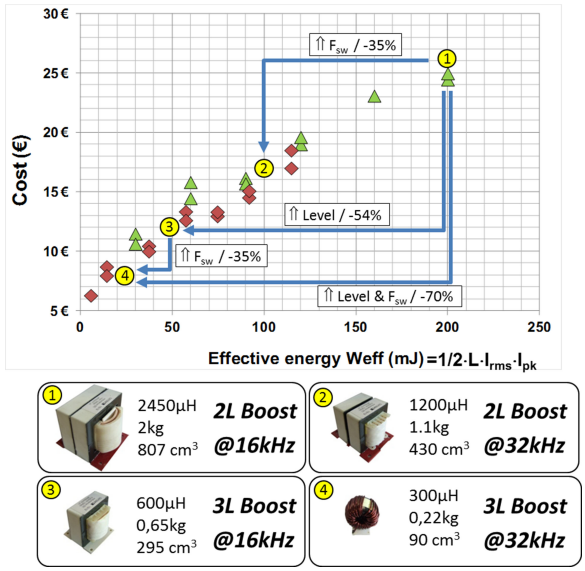

Fig. 1. Cost comparison of inductor for various switching frequencies.

The motivation for this paper is to present the design of a low cost and highly efficient front-end boost converter for single-phase grid-tied inverters [10]–[12]. As a cost-effective alternative to WBG devices, a multilevel approach using Si components is proposed. To cope with their intrinsic limitations, an original design method is proposed which allows partially achieving soft switching.

This paper is organized as follows. In Section II, a short overview of step-up topologies is done, permitting us to select an optimum topology, in the light of the discussion above. The functional analysis of the selected topology is given in Section III. Sections IV and V investigate a novel lossless snubber applied to the selected topology and its design. Experimental results are shown in Section VI.

II. Overview of Transformerless Step-Up Topologies

The conventional boost is the basic topology to step-up voltage without requiring a transformer. In spite of an affordable

Manuscript received January 7, 2015; revised March 12, 2015 and May 4, 2015; accepted May 11, 2015. Date of publication June 24, 2015; date of current version November 16, 2015. Recommended for publication by Associate Editor G. Moschopoulos.

The authors are with the Mitsubishi Electric Research Center Europe, Rennes 35700, France (e-mail: lefevre.gc@free.fr; s.mollov@fr.merce.mee.com).

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Digital Object Identifier 10.1109/TPEL.2015.2438036

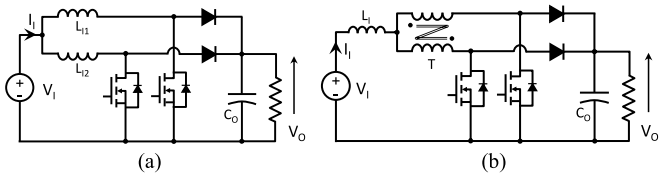

Fig. 2. (a) Interleaved boost. (b) Three-level transformer-based boost.

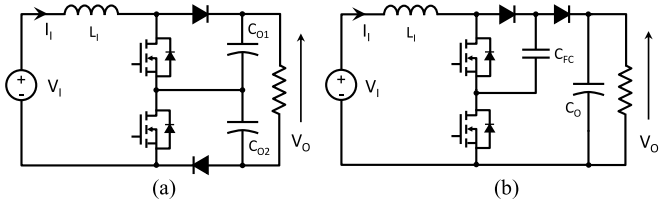

Fig. 3. (a) Three-level boost. (b) Three-level FC boost topology.

complexity, differential mode (DM) filtering requirements are high and efficiency cannot reach very high levels [13]. Derived from the previous architecture, the interleaved boost consists of two switching cells (transistor/diode) as depicted in Fig. 2(a). More than simply halving current constraints, the main advantage is to operate with an apparent frequency of $2{\cdot}F_{\rm SW}$ due to 180° phase shift between the legs. This interleaving technique not only benefits the design of both input and output capacitive banks but also reduces the input current ripple or even cancels it for operations at 50% duty ratio. However, the total magnetic energy remains unchanged for a given current swing in the switches. To further reduce the requirements on the input storage, a three-level version can be achieved by using a transformer [see Fig. 2(b)], e.g., [13]. Nevertheless, the voltage to which the active devices are exposed is the output voltage.

To reduce the voltage stress on devices, three-level and flying-capacitor (FC) boost converters [14], [15] can be used as depicted in Fig. 3. With interleaved control signals and due to an additional voltage level, the inductor value is reduced by a factor of 4 with regards to the conventional boost [14]. Irrespective of the switching frequency, the losses and the cost are reduced compared to a two-level topology [8].

Three-level topologies outperform two-level topologies only if reducing the voltage constraints [16] allows the use of suitable voltage class devices. Otherwise, switching losses are almost similar, while static performance is degraded due to series device connection. Depending on the voltage range of the dc bus, these topologies cannot make full use of low-loss devices, even with rated voltages divided by 2. The only way to overcome this limitation is to unbalance the design, by applying asymmetric voltage constraints for the switching cells. Hence, the static and dynamic performances of one switching cell can be optimized by implementing low-voltage devices. The other cell can be assisted with an adequate circuit performing zero-voltage switching (ZVS) or zero-current switching (ZCS).

TABLE I
PERFORMANCES OF BEST-IN-CLASS 250/300 AND 650-V COMPONENTS

	Rated Current $I_{\rm FWD}$ [A]	Forward voltage at $I_{\rm FWD}$ [V]	$Q_{\rm rr}$ at $I_{\rm FWD}$, (1kA/μs) [nC]
300-V Si Diode	15	0.85	200
600-V Si Diode	15	1.1	800
	Specific resistance $[\Omega \cdot {\rm cm}^2]$	Specific gate charge $Q_{\rm GD}$, $V_{\rm GS} = 10$ V [nC/cm^2]	
250-V MOSFET	≈ 6.5 ($A = 32$ mm^2)	22	
650-V MOSFET	≈ 12 (A = 27 mm^2)	110	

III. FUNCTIONAL ANALYSIS OF THE ASYMMETRIC FC BOOST CONVERTER

A. Motivation

For a dc-link voltage around 400 V, only switches withstanding at least 300 V can be selected in a three-level topology. Unfortunately, the current developments in the field of semiconductors rather promote 600-V MOSFETs and IGBTs, in particular due to single-switch topologies. This trend also remains true for technologies of fast diodes. However, with an asymmetric design, 250-V devices can be advantageously selected in the FC's switching cell to operate safely.

To better understand the motivation of implementing 250/300 V instead of 600-V devices, Table I gives an overview of the currently best-in-class components. The forward voltage V_f as well as the recovery charge $Q_{\rm rr}$ are used as performance indicator for diodes, whereas specific resistance ($\Omega \cdot {\rm cm}^2$) and gate-to-drain charge $Q_{\rm GD}$ (${\rm nC}/{\rm cm}^2$) are more relevant for MOSFETs.

From Table I, the 300-V diodes have much better dynamic performances, with the gain being less significant in terms of static characteristics. This trend remains true for MOSFET even if the specific resistance of the latest 600-V superjunction (SJ) devices is outstanding. The dynamic performance is still below low-voltage devices despite manufacturers' efforts to reduce parasitic capacitances [17], [18].

We propose to incorporate both technologies in the three-level boost topology: use low-voltage MOSFETs for the flying-capacitor cell and enhance the dynamic performances of the high-voltage MOSFETs with a dedicated soft-switching circuit.

The purpose of this section is, therefore, to demonstrate the advantage of an unbalanced FC operation and to derive the associated voltage control.

B. Analysis of Steady-State Operations

Fig. 4 summarizes the different switching combinations of ${\rm M}_1$ and ${\rm M}_2$ and the associated topological configurations. The sequences II and IV are involved in the FC charge and discharge process, whereas the FC is bypassed during the configurations I and III.

In the ideal case of a lossless converter with ripple-free state-variables (V_O, $V_{\rm FC}$, V_i, and I_i), those sequences are naturally balanced for similar conduction times of ${\rm M}_1$ and ${\rm M}_2$ during

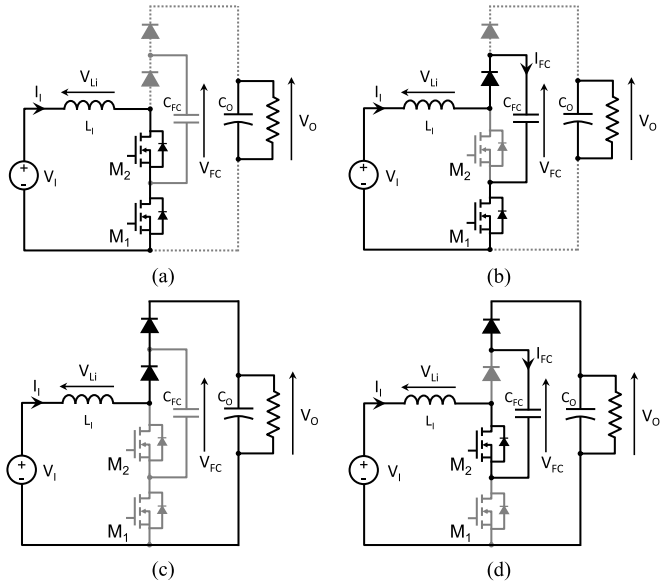

Fig. 4. (a) Configuration I. (b) Configuration II. (c) Configuration III. (d) Configuration IV.

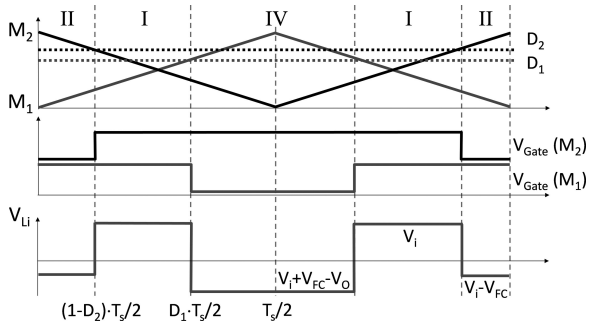

Fig. 5. PWM waveforms, switching states sequence, and voltage across the filtering inductor for $D_1 + D_2 \geq 1$.

steady-state operations [19], [20]. With classical condition of $V_O = V_{\rm FC}/2$, the duty cycle mismatch between switches is usually negligible, in particular in continuous-current mode and small current ripples [20]. Here, two duty cycles D_1 and D_2 are, however, considered since the motivation is to investigate the operation with $V_O \neq V_{\rm FC}/2$. Two modes can occur depending on whether overlapping exists between channels ($D_1 + D_2 \geq 1$) or not ($D_1 + D_2 \leq 1$). Fig. 5 describes the overlapping case, the evolution of the state-variables in the other mode being determined by symmetry.

Based on the waveforms of Fig. 5, the average inductor voltage V_{Li} over a switching period is

$$\begin{aligned}\langle V_{Li}\rangle_{T\rm sw} &= \left(\frac{1-D_2}{2}\right)\cdot(V_I - V_{\rm FC}) \\ &+ \left(\frac{D_1+D_2-1}{2}\right)\cdot V_I + \left(\frac{1-D_1}{2}\right) \\ &\cdot(V_I + V_{\rm FC} - V_O)\,. \end{aligned} \tag{1}$$

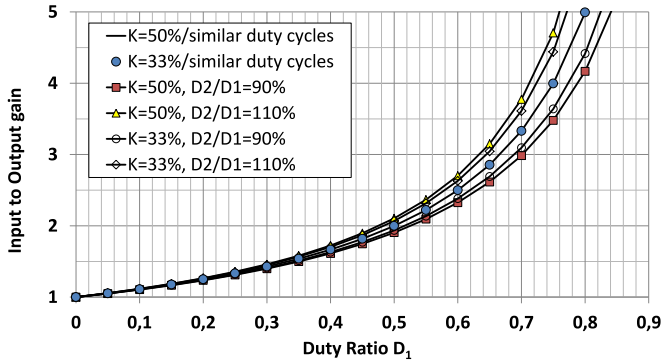

Fig. 6. Boost theoretical gain with arbitrary parameters.

Steady-state operation implies that the average voltage on L_i is null. Using the convention $K = V_{\rm FC}/V_O$ and $\beta = D_2/D_1$, the boost voltage gain is calculated according to

$$\frac{V_O}{V_I} = \frac{1}{1 - D_1\cdot(1 - K\cdot(1-\beta))}. \tag{2}$$

Equation (2) is plotted in Fig. 6 for $K = \{1/2 \text{ or } 1/3\}$ and $\beta = \{0, 9/1, 1\}$. For equal values of D_1 and D_2, the converter behaves as a standard boost and $V_{\rm FC}$ can be arbitrary chosen without affecting the conversion gain (the two curves completely overlap). The impact of differing D_1 and D_2 is small, except for extremely high duty cycles. To sum up, this topology can be seen as a conventional boost controlled by a single duty cycle $D = D_1 = D_2$ even if the FC cell voltage is different from $V_O/2$.

C. Analysis of the Current Ripple

As with most dual-interleaved or three-level converters, an inductor-ripple-free current can be generated with a duty cycle $D = 0,5$. In the three-level FC converter, this only occurs due to the $180\circ$ phase shift between the two switching cells and if the voltage across the FC perfectly matches half the output voltage. From steady-state waveforms, the current ripple (normalised to its dc component) can be easily derived for a conventional two-level (2L) boost converters (3), (4) as well as for a three-level (3L) FC boost converter (5) with $V_{\rm FC} = V_O/2$ [21]

$$\Delta I_{\rm R,max} = \frac{\Delta I_{\rm pk}}{I_I} = \frac{V_O}{4\cdot L_I\cdot f_{\rm sw}\cdot I_I} \tag{3}$$

$$\Delta I_{R,2\rm L} = 4\cdot D\cdot(1-D)\cdot\Delta I_{R,\rm max} \tag{4}$$

$$\Delta I_{R,3\rm L} = 2\cdot(2\cdot D - 1)\cdot\Delta I_{R,\rm max} \cdot\begin{cases} -D, & \text{if} \quad D \leq 0.5 \\ (1-D)\,, & \text{if} \quad D \geq 0.5\,. \end{cases} \tag{5}$$

According to the discussion in Section III-A, only the condition $V_{\rm FC} \leq V_O/2$ is of interest, for which the current ripple can be easily computed from.

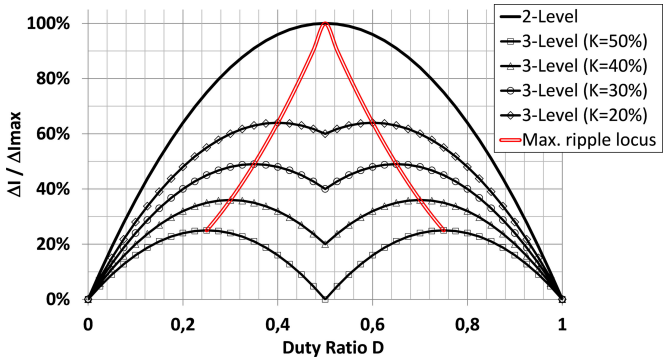

Fig. 7. Comparison of ripple functions between two-level and three-level boost converters for different *K* factors.

$$\Delta I^*_{R,3\mathrm{L}} = 4 \cdot \Delta I_{R,\max} \cdot \begin{cases} D \cdot (1-K-D), & \text{if} \quad D \le 0.5 \\ (1-D) \cdot (D-K), & \text{if} \quad D \ge 0.5. \end{cases} \tag{6}$$

Fig. 7 shows the typical profiles of the peak input ripple against the duty ratio *D* for the studied cases.

From (6), the maximum ripple can be defined for an arbitrary value of *K* factor as

$$D_{\mathrm{worst}} = \frac{1-K}{2} \tag{7}$$

$$\Delta I^*_{R-\mathrm{worst}} = \Delta I^*_{R,3\mathrm{L}}\left(D_{\mathrm{worst}}\right) = (1-K)^2 \cdot \Delta I_{R,\max}. \tag{8}$$

The FC voltage can be selected to fit a given semiconductor technology or increase the safety margin. This is paid by an increase of the storage requirements, though for moderate deviations around $K = 0.5$, the relative current ripple remains low.

IV. Improvements to Achieve Soft-Switching Features

As mentioned in Section III, there are no significant improvements to consider to further enhance the converter performance beyond the use of the 250/300-V devices. Consequently, the FC's cell optimization is out of the scope of this paper and only the principal switching cell including M_1 and diode D is considered. To achieve this goal, a novel ZVZCS snubber (EP2782235 A1) is proposed [22].

A. ZVS/ZCS Soft-Switching Transitions on the Main Switches

The topology is extended to complete soft-switching operations (ZVS, ZCS) by adding an inductor L_{SN} and two capacitors C_{SN1} and C_{SN2} associated with diodes $\mathrm{D}_{\mathrm{SN1}}$ and $\mathrm{D}_{\mathrm{SN2}}$ as depicted in Fig. 8. The concept can be generalized for an arbitrary number of levels as shown in Fig. 9. Keep in mind that the inner FC cell operates under hard switching.

The use of split capacitors is not mandatory but goes along with a reduced stray inductance between semiconductors and snubber capacitors and helps reduce overvoltages. Moreover, current constraints are equitably shared.

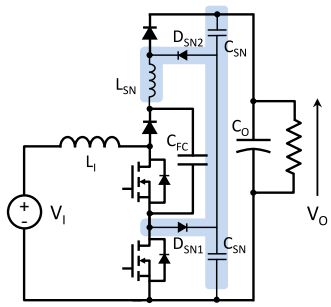

Fig. 8. Proposed arrangement to achieve ZVS/ZCS transitions.

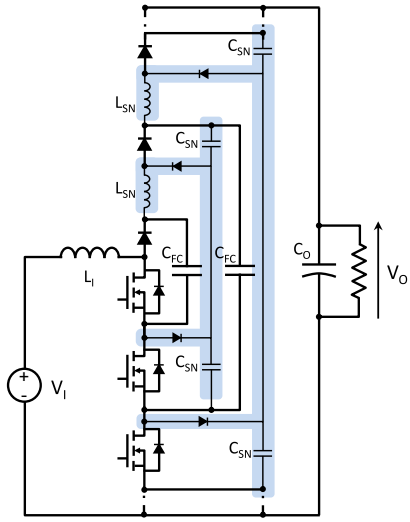

Fig. 9. Extension to an arbitrary number of levels.

The snubber inductor can be either located in series with the switch or with the freewheeling diode. The maximum boost ratio is directly capped by the losses for large duty ratios, basically those located in the branch including the switch and the filtering inductor [21]. Also, in order to reduce the overall cost due to gate driving, the inductor is advantageously mounted in series with the diode. It must be pointed out that L_{SN} can be split into two coupled chokes implemented in both positions. Even if the advantage is not trivial, this solution can facilitate the use of PCB integrated inductors.

B. Advantages of the Proposed Snubber

The basic benefits of using the snubber are:

1) ZCS/ZVS features: losses in the switch and the diode are nearly cancelled for both turn-on and turn-off transitions;
2) *dI/dt* control: the recovery charge Q_{RR} is reduced as well as the peak current I_{RR}. Far more than reducing the dissipated energy, global EMI behavior is undeniably enhanced;
3) *dV/dt* control: improved CM spectrum and reduction of recovery losses in the freewheeling diode due to the fact that voltage remains low after the recovery peak is reached. This is even more significant with snappy diodes;

4) all charge/discharge processes are nondissipative;
5) locating the snubber inductor as suggested implies a better use of the magnetic core. In particular during turn-on, the resonant current in $L_{\rm SN}$ does not superimpose on the input current. Both magnetic quadrants are used and the saturation field is set with regard to max (I_I, $I_{\rm PK}$);
6) implement synchronous rectification (SR) more easily. As claimed first, shoot-through is naturally prevented since the snubber inductor is in series with semiconductors.

V. Analysis of the Proposed Lossless Snubber

In this section, the operation of the lossless snubber is described. First, it is supposed that:

1) the input current is filtered and equals I_I; the output voltage V_O and $V_{\rm FC}$ are ripple-free;
2) parasitic capacitances of the components are constant and small enough to be neglected compared to $C_{\rm SN1} + C_{\rm SN2} = C_{\rm SN}$ during resonances; the relevancy of this claim, more especially with SJ devices, will be discussed later on;
3) the diode is recovery-free under ZCS conditions, due to the low *dI/dt* and intrinsic performances of the latest generation of fast diodes.

For illustrative purposes, the FC cell is replaced by a voltage source, showing operation for $D \leq 0.5$, though the analysis is applicable for any duty cycle. The angular frequency and characteristic impedance for the snubber are

$$\omega_R = \frac{1}{\sqrt{L_{\rm SN} \cdot C_{\rm SN}}}, \qquad Z_C = \sqrt{\frac{L_{\rm SN}}{C_{\rm SN}}}. \tag{9}$$

A. Turn-On Transitions

The successive stages during turn-on transitions are given in Fig. 10. The blue arrow is related to reactive energy transfer between the snubber elements, regardless of the effective power transfer from input to output, symbolized in red. The principal snubber waveforms are displayed in Fig. 11.

1) Stage n°1*: Linear Discharge of* $L_{\rm SN}$*:* $\rm M_1$ is turned ON. Due to the presence of $L_{\rm SN}$ in series inside the switching cell, the voltage drops to zero without any previous Miller phase and the MOSFET channel is immediately conductive. The parasitic capacitance $C_{\rm OSS}$ discharges in the channel and, simultaneously, the currents in $L_{\rm SN}$ and $\rm M_1$ start evolving according to

$$L_{\rm SN} \cdot \frac{dI_{L\rm sn}}{dt} = -(V_O - V_{\rm FC}) \tag{10}$$

$$I_{(M1)}(t) = \frac{V_O - V_{\rm FC}}{L_{\rm SN}} \cdot t. \tag{11}$$

During that time, the diode $\rm D_{SN1}$ remains blocked since the voltage across $C_{\rm SN1}$ is higher than the on-state voltage of $\rm M_1$, even in case of partial ZVS. The duration of Stage n°1 is

$$\Delta t_1 = \frac{L_{\rm SN} \cdot I_I}{V_O - V_{\rm FC}}. \tag{12}$$

Note that this stage does not exist for DCM. In case of non-negligible recovery, this stage is slightly longer and lasts until the peak current recovery is reached. Once the current through the diode D cancels, a reverse voltage can be applied across its terminals.

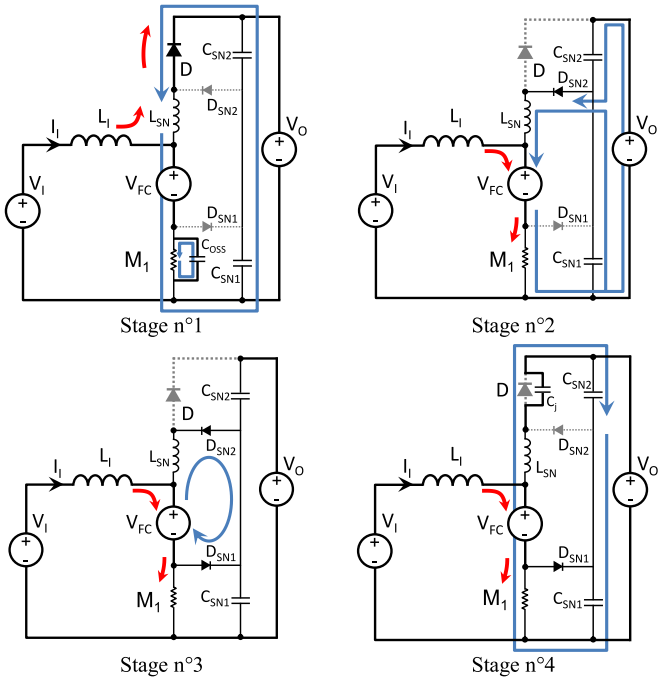

Fig. 10. Description of the topological configurations during turn-on.

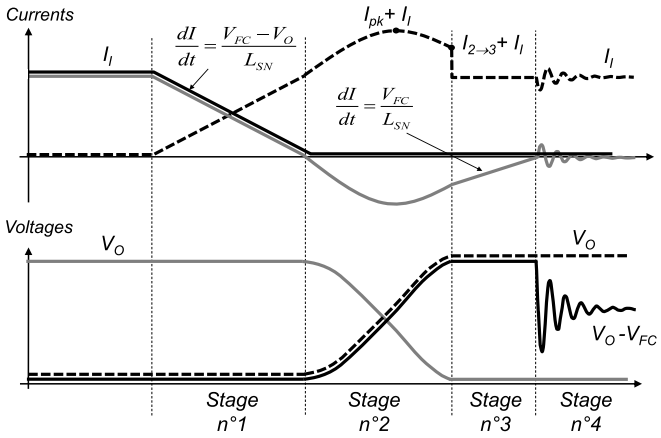

Fig. 11. Principal waveforms with the proposed lossless snubber. Currents : D (black), $\rm M_1$ (dashed) and $L_{\rm SN}$ (gray). Voltages : D (black), capacitors $C_{\rm SN1}$ (gray) and $C_{\rm SN2}$ (dashed).

2) Stage n°2*: Resonant Mode:* A resonance occurs between the snubber elements based on the following initial conditions:

$$I_{L\rm sn} = 0, \quad V_{C\rm sn1} = V_O, \quad V_{C\rm sn2} = 0 \tag{13}$$

$$I_{L\rm sn}(t) = I_{\rm PK} \cdot \sin(\omega_R \cdot t) \tag{14}$$

with $I_{\rm PK} = (V_O - V_{\rm FC})/Z_C$

$$V_D(t) = (V_O - V_{\rm FC}) \cdot (1 - \cos(\omega_R \cdot t)). \tag{15}$$

In order to achieve the complete discharge of the bottom snubber capacitor $C_{\rm SN1}$, thus ensuring full ZVS on $\rm M_1$ during turn-off, the output voltage V_O must be at least twice higher

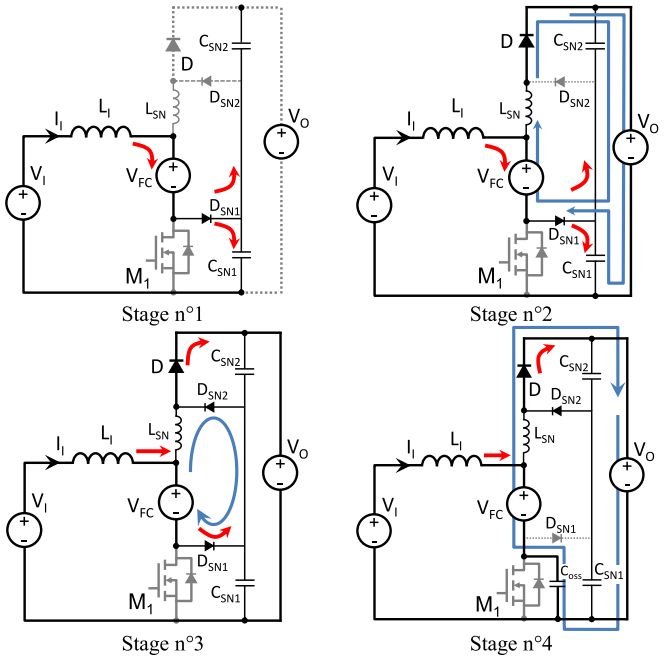

Fig. 12. Description of the topological configurations during turn-off.

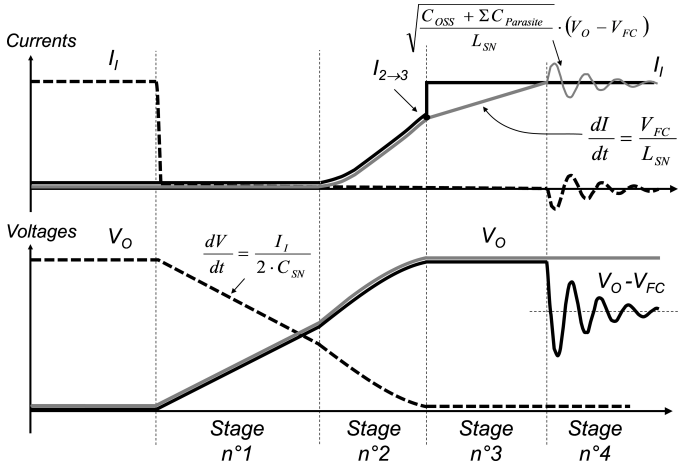

Fig. 13. Principal waveforms with the proposed lossless snubber. Currents : D (black), M_1 (dashed) and L_{SN} (gray). Voltages : M_1 (black), capacitors $C_{\mathrm{SN}1}$ (gray) and $C_{\mathrm{SN}2}$ (dashed).

than V_{FC}. This is an interesting result because with the proposed approach, this condition is naturally fulfilled.

At the end of Stage n°2, the voltage across the diode D is V_O and the current flowing through L_{SN} is

$$I_{2\to3} = Z_C \cdot \sqrt{(V_0 - V_{\mathrm{FC}})^2 - V_{\mathrm{FC}}^2}. \tag{16}$$

Finally, $\mathrm{D}_{\mathrm{SN}1}$ gets conductive and Stage n°3 begins.

3) Stage n°3*: Full Discharge of* L_{SN} *Via the FC:* Both $\mathrm{D}_{\mathrm{SN}1}$ and $\mathrm{D}_{\mathrm{SN}2}$ are conductive. The voltage V_{FC} is applied on L_{SN} which is finally demagnetised according to

$$L_{\mathrm{SN}} \cdot \frac{dI_{L\mathrm{sn}}}{dt} = V_{\mathrm{FC}}. \tag{17}$$

4) Stage n°4*: Resonance Involving* L_{SN} *and* C_J*:* As soon as the current cancels in L_{SN}, $\mathrm{D}_{\mathrm{SN}2}$ gets blocked and a resonance starts between L_{SN} and the diode's junction capacitance C_J to reach the steady-state reverse blocked voltage $V_0 - V_{\mathrm{FC}}$ across the diode.

B. Tutn-Off Transitions

The successive stages during the turn-off transitions are given in Fig. 12 with the corresponding waveforms in Fig. 13.

1) Stage n°1*: Linear Charge of* $C_{\mathrm{SN}1}$*/Discharge of* $C_{\mathrm{SN}2}$*:* M_1 is turned OFF. Since the main diode D is still blocked, $\mathrm{D}_{\mathrm{SN}1}$ gets conductive and the current flows through the snubber capacitors $C_{\mathrm{SN}1}$ and $C_{\mathrm{SN}2}$, defining the ZVS transition

$$I_I = C_{\mathrm{SN}1} \cdot \frac{dV_{C\mathrm{sn}1}}{dt} + C_{\mathrm{SN}2} \cdot \frac{dV_{C\mathrm{sn}2}}{dt}. \tag{18}$$

Meanwhile, the voltage across the diode decreases as in

$$V_D(t) = V_O - V_{\mathrm{FC}} - \frac{I_I}{C_{\mathrm{SN}}} \cdot t. \tag{19}$$

When $V_D = 0$, a new stage begins.

2) Stage n°2*: Resonant Mode:* A resonance occurs between the snubber elements. In parallel to the previous charging/discharging mode (depicted with red arrows in Fig. 12), a resonant current flows in the branch including L_{SN}, $C_{\mathrm{SN}1}$, $C_{\mathrm{SN}2}$ as well as the freewheeling diode D and the two voltages sources V_O and V_{FC}. The waveform trajectories and their initial conditions are

$$I_{L\mathrm{sn}} = 0, \quad V_{C\mathrm{sn}1} = V_O - V_{\mathrm{FC}}, \quad V_{C\mathrm{sn}2} = V_{\mathrm{FC}} \tag{20}$$

$$V_{C\mathrm{sn}1}(t) = (V_O - V_{\mathrm{FC}}) + Z_C \cdot I_I \cdot \sin(\omega_R \cdot t) \tag{21}$$

$$I_{L\mathrm{sn}}(t) = I_I \cdot (1 - \cos(\omega_R \cdot t)). \tag{22}$$

This stage continues until the diode $\mathrm{D}_{\mathrm{SN}2}$ gets conductive when $V_{C\mathrm{sn}2} = 0$. However, the resonance may stop if the inductor L_{SN} is fully charged ($I_{L\mathrm{sn}} = I_I$) before half the resonant period, i.e., if the electromagnetic energy is lower than the electrostatic energy. Then, the initial conditions selected during the resonant mode at turn-on are different and only partial ZVS is possible for the freewheeling diode D. This also comes along with modified steady-state values for $V_{C\mathrm{sn}1}$ and $V_{C\mathrm{sn}2}$ and consequently partial ZVS on M_1 during turn-off. For the sake of simplicity, this case is not investigated in this section and the electromagnetic energy W_{MAG} is assumed to be higher than the electrostatic energy W_{CAP}. Therefore

$$\frac{1}{2} \cdot L_{\mathrm{SN}} \cdot I_I^2 \geq \frac{1}{2} \cdot C_{\mathrm{SN}} \cdot V_{\mathrm{FC}}^2. \tag{23}$$

The duration of Stage n°2 is

$$t_{2\to3} = \frac{1}{\omega_R} \cdot \arcsin\left(\frac{V_{\mathrm{FC}}}{Z_C \cdot I_I}\right). \tag{24}$$

Finally, $\mathrm{D}_{\mathrm{SN}2}$ gets conductive and Stage n°3 begins. At the end of Stage n°2, the voltage applied across M_1 is V_O and the current flowing through L_{SN} is

$$I_{2\to3} = I_I \cdot \left(1 - \sqrt{1 - \frac{W_{CAP}}{W_{\mathrm{MAG}}}}\right). \tag{25}$$

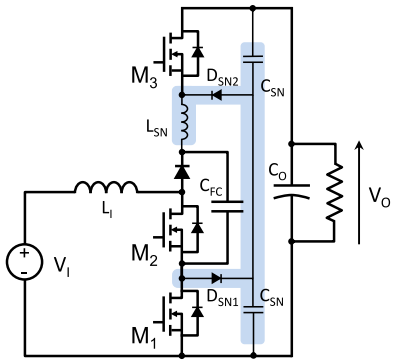

Fig. 14. Topology using the proposed snubber and SR between M_1 and M_3.

3) Stage n°3*: Full Recharge of* L_{SN} *Via the FC:* Both $\mathrm{D}_{\mathrm{SN}1}$ and $\mathrm{D}_{\mathrm{SN}2}$ are conductive. The voltage V_{FC} is applied on L_{SN} which finishes to charge up to I_I

$$I_{L\mathrm{sn}}(t) = I_{2\to 3} + \frac{V_{\mathrm{FC}}}{L_{\mathrm{SN}}} \cdot t. \tag{26}$$

4) Stage n°4*: Resonance Involving* L_{SN} *and* C_{OSS}*:* As soon as the current in L_{SN} equals I_I, $\mathrm{D}_{\mathrm{SN}1}$ gets blocked and a resonance occurs between L_{SN} and the parasitic capacitance C_{OSS}. The steady-state blocked voltage is $V_0 - V_{\mathrm{FC}}$. During this resonance, not only C_{OSS} resonates but also all the devices with floating potentials like the FC cell for instance. The corresponding peak current is a good way to estimate their respective value.

VI. Implementation of SR

A. Challenges

The motivations for implementing SR, as depicted in Fig. 14, are:

1) to further improve the on-state performances of the freewheeling diode D by operating a MOSFET in the third quadrant (conductive channel with negative current) and intend to reach similar performances to low-voltage components (typically 250/300 V);
2) to potentially demonstrate the effectiveness of the snubber with two controlled switches, especially SJ MOSFETs and open new perspectives in inverters or rectifiers.

The main limitation of MOSFETs is the intrinsic body diode stemming from the p^+-n^--n^+ internal structure of the component [23]. Despites acceptable conduction performances, the dynamic performances as well as the *dV/dt* ruggedness are very poor. Even with low *dI/dt* (around 50 A/μs), it is common to deal with a recovered charge of several microcoulombs. By minimizing the diode's conduction time, the reverse recovery can be significantly reduced by dead time optimization [23], [24]. However, special circuitry is necessary to adjust the duration without affecting safety. Other solutions consist of deriving the current in auxiliary branches for instance [25]–[27]. This completely addresses the recovery issue but requires additional devices. With the proposed snubber, the reverse recovery effects are intrinsically mitigated because of controlled *dI/dt* and *dV/dt*. Recovery-related losses can be further lowered by properly adjusting dead times between switches M_1 and M_3, keeping in mind that shoot-through is prevented. This section discusses the appropriate control taking full advantage of the snubber presented in the previous section, while minimizing the snubber constraints.

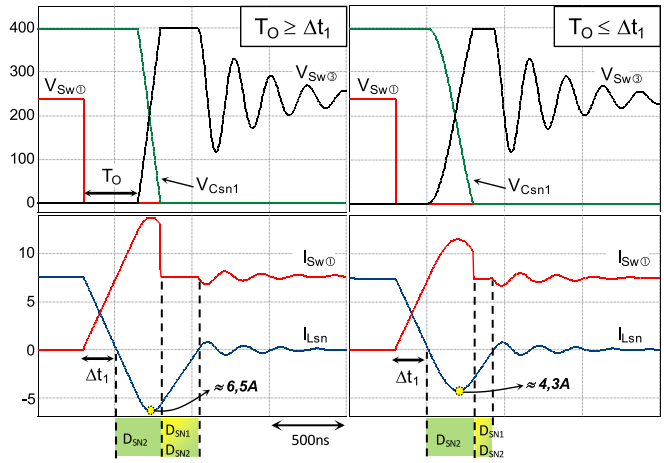

Fig. 15. Simulated turn-on waveforms for various overlapping times T_O. [top traces: Voltages (V), bottom traces: Currents (A)].

TABLE II
Electrical Parameters and Components Values

Parameter	Value
Input voltage V_I	234 V
Output voltage V_O	400 V
FC voltage V_{FC}	160 V ($K = 0.4$)
Average input current	8.5 A
Snubber elements C_{SN}, L_{SN}	2 nF / 6.8 μH

B. Turn-On Transitions

With conventional dead time, operations are unchanged compared to a freewheeling diode. However, an overlapping time T_O (between M_1 and M_3) can also be selected since M_3 remains conductive during the discharge of L_{SN}, after M_1 turns ON. Depending on T_O, two cases may occur. Fig. 15 shows comparative simulation results, with an arbitrary overlapping of 400 ns. The associated electrical parameters and the components values are shown in Table II.

1) Overlapping Time T_O *is Lower Than* Δt_1*:* M_3 is turned OFF before the current completely cancels and its body diode gets conductive. However, the required time Δt_1 to discharge L_{SN} is directly proportional to the current level and a dynamic adjustment may be necessary to optimally bypass the diode. Either T_D is automatically adjusted for a given current or no dead times are implemented. In the last case, the diode's conduction time cannot exceed $\Delta t_1(I_{\max})$.

2) Overlapping Time T_O *is Higher Than* Δt_1*:* Even after $I_{L\mathrm{sn}}$ has been cancelled, M_3 remains conductive, a shoot-through mode occurs (M_1 and M_3 conductive) and the resonance with C_{SN} is blocked. The current sign reverses and the current in L_{SN} keeps decreasing till the effective turn-off. The current

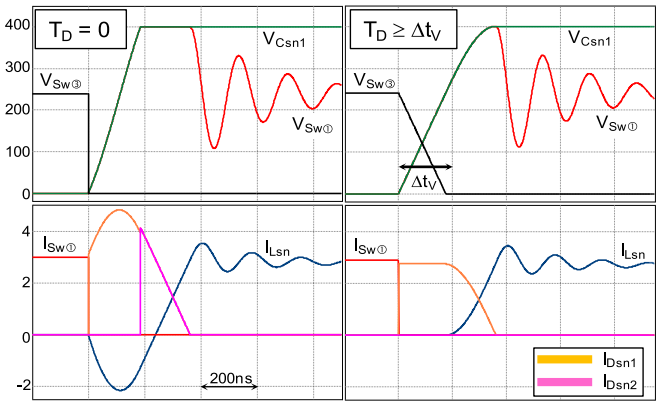

Fig. 16. Simulated turn-off waveforms for two limit cases of dead time T_D. [top traces: Voltages (V), bottom traces: Currents (A)].

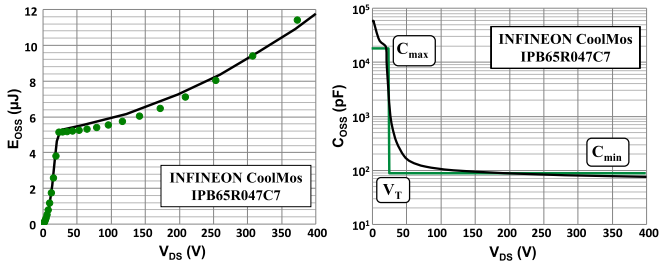

Fig. 17. Equivalent model of Coss for the selected SJ MOSFET with the parameters: $C_{\max} = 17$ nF, $C_{\min} = 88$ pF, and $V_T = 25$ V.

constraints on $L_{\rm SN}$, $\rm D_{SN\,1}$, as well as $\rm D_{SN\,2}$ are thus significantly increased. At light loads, an excess of reactive energy circulates, yielding additional losses.

C. Turn-Off Transitions

Turning-on $\rm M_3$ without completely discharging the capacitor $C_{\rm SN2}$ is critical since

1) the parasitic capacitance $C_{\rm OSS}$ of $\rm M_3$ is discharged through the channel, thus dissipating $E_{\rm OSS}\cdot f_{\rm SW}$, whereas it is possible to perform a lossless discharge;
2) $\rm M_3$ is immediately conductive, the Stages n°1 and 2 (linear charge/discharge of $C_{\rm SN}$ then resonance) are replaced with a unique resonant sequence. It can be easily demonstrated that the condition to achieve the complete charge/discharge of $C_{\rm SN}$ and achieve ZVS on $\rm M_3$ during turn-on is $V_O \geq 2\cdot V_{\rm FC}$, regardless of the current value. Though the extended ZVS range appears as an advantage, the conduction losses stemming from circulating energy along with the discharge of $C_{\rm OSS}$ diminish the part-load efficiency.

Simulation results in Fig. 16 illustrate the energy flow at the ZVS range boundary (2.7 A with the selected values) with dead time of zero and 200 ns. The ZVS range extension is clearly visible, the voltage across the snubber reaching its final value much before the current cancels in the snubber diodes. The current constraints on the diodes are significantly increased as well as the high-frequency copper and core losses in the snubber inductor due to an additional resonance (negative current).

VII. Design Guidelines

In this section, the design procedure of the converter is presented. The main components requiring attention are the input inductor and the snubber elements.

According to the specification, the boost converter operates with an output voltage V_O in the range [270–400 V] assuming that the dc/ac stage uses a bipolar PWM with a maximum modulation depth of 90%. Under nominal conditions, the dc-link voltage is $V_{\rm nom} = 330$ V. To avoid destroying the devices in the FC cell, the FC voltage is set as

$$V_{\rm FC} = \min\left(\frac{V_O}{2}, \frac{V_{\rm nom}}{2}\right). \tag{27}$$

A. Design of the Input Inductor

With the results of Section II, the relative peak to peak ripple (in%) for a given value of *K* factor is

$$\Delta I^{\%}_{\rm pk-pk} = (1-K_{\min})^2 \cdot \frac{V_{O\,\max}}{4\cdot L_I \cdot f_{\rm sw}\cdot I_I}. \tag{28}$$

Because the *K* factor is minimum at high output voltage, one can define the required impedance in the worst case

$$Z_L = \left(1-\frac{V_{\rm nom}}{2\cdot V_{O\,\max}}\right)^2 \cdot \frac{V_{O\,\max}}{4\cdot \Delta I^{\%}_{\rm pk-pk}\cdot I_I}. \tag{29}$$

Limiting $\Delta I\%_{\rm pk-pk}$ to 30% under nominal conditions requires an inductor of 270 μH with a switching frequency of 30 kHz.

B. Design of the Snubber Capacitor

The device intrinsic output capacitance $C_{\rm OSS}$ can help achieve pseudo-ZVS [18]. External capacitors $C_{\rm SN}$ are used to further decrease the switching losses, reduce *dV/dt* and mask the $C_{\rm OSS}$ nonlinearity with voltage. To model the capacitive behavior of SJ devices, two values $C_{\min}$ and $C_{\max}$ as well as a transition voltage V_T are used. This model directly stems from the physical insight of the SJ capacitance modulation [17], [18]. A least-mean-square fit is used to define the parameters from the energy $E_{\rm OSS}$ as in Fig. 17.

Based on [18] with $I = 8.5$ A, the turn-off *dI/dt* and *dV/dt* for C7-generation MOSFETs are roughly 500 A/μs and 25 V/ns regardless of the gate resistance. If the voltage rise time is similar to the current fall time ($\approx$ 17 ns), the losses with a capacitive snubber are theoretically divided by a factor of 6.

The corresponding external capacitor under nominal conditions is

$$C_{\rm SN} = \frac{I_{I\_\max}\cdot t_{\rm fall\_I}}{V_O - V_{\rm FC}} - C_{\rm OSS} \approx 500\ \text{pF} \tag{30}$$

with $V_0 = 330$ V and $V_{\rm FC} = 165$ V.

The voltage rise rate is though reduced by a factor of 2 which is judged to be still aggressive in EMI terms. To get a safety

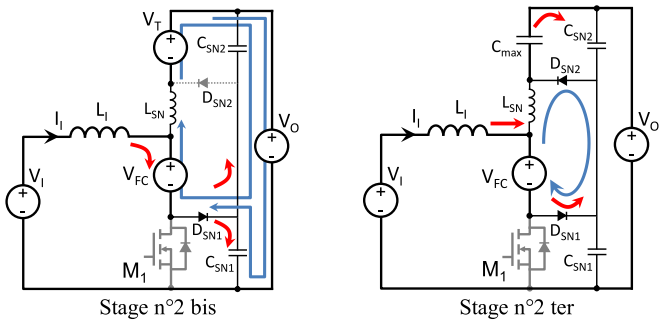

Fig. 18. Intermediate topological configurations with parasitic capacitors.

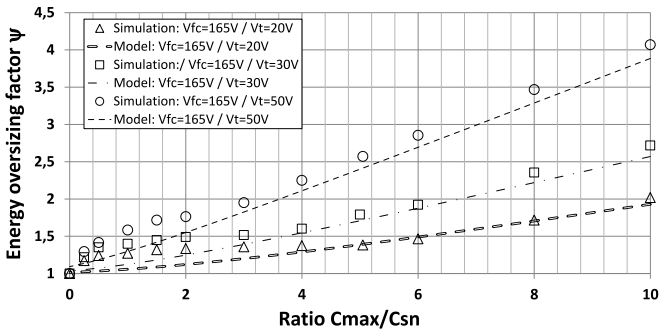

Fig. 19. Comparative results of simulations and proposed analytical model for the energy oversizing factor ψ.

margin and lower the voltage rise rate, two ceramic capacitors (C0 G) of 1 nF were eventually selected.

To understand the effect of nonlinear capacitance introduced by the SJ MOSFET, a nonlinearity factor Ψ is defined, representing the ratio between the full-recharge energies for linear and nonlinear snubber capacitors. To derive analytical formulas for Ψ, it was supposed that $C_{\max} >> C_{\rm SN} >> C_{\min}$. In case of resonance involving $C_{\rm SN}$, $\rm M_3$ is modeled as an open circuit for $V \geq V_T$ or a voltage source at V_T otherwise. The analysis in Section V was, thus, refined by dividing the Stage n°2 into two subintervals with configurations shown in Fig. 18.

From this model, the closed-form solution for Ψ is

$$\Psi = \frac{2\left(\left(1+\frac{C_{\max}}{C_{\rm SN}}\right)\cdot\frac{V_T}{V_{\rm FC}}\right)^2}{-1+\sqrt{1+4\cdot\left(\left(1+\frac{C_{\max}}{C_{\rm SN}}\right)\cdot\frac{V_T}{V_{\rm FC}}\right)^2}}. \quad (31)$$

Fig. 19 plots the model of (31) and discrete points from a time-domain simulation. The accuracy of (31) is satisfactory, with largest errors seen for small $C_{\max}/C_{\rm sn}$ ratios, indicating that (31) somewhat prioritizes the nonlinearity effect.

C. Design of the Snubber Inductor

As mentioned in Section IV, the ZVS range directly derives from the balance between snubber electrostatic and magnetic energies, with larger $L_{\rm SN}$ resulting in extended ZVS load range. However, large snubber inductors result in excessive losses in

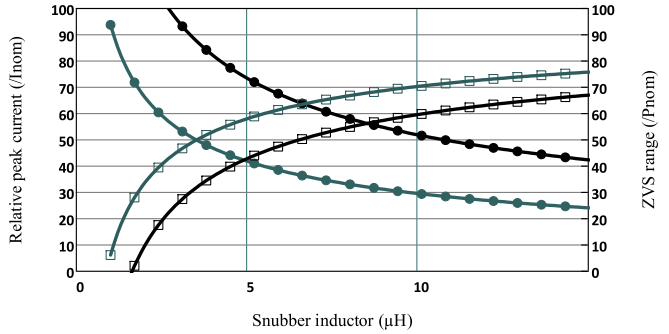

Fig. 20. Design constraints ($I_{\rm pk}$ and ZVS range) for the snubber inductor. $I_{\rm pk}$ (round markers): freewheeling diode (gray), SR MOS (black). ZVS range (square markers): freewheeling diode (gray), SR MOS (black).

the inductor and the diodes $\rm D_{SN1\&2}$. On the other hand, small values of $L_{\rm SN}$ permit large current spikes occurring during turn-on transitions which might saturate the magnetic material. In order to accurately predict the requirements on $L_{\rm SN}$, a more complex approach taking into account parasitic capacitors $C_{\rm OSS}$ is presented. Based on the capacitive model of SJ devices, an analytical derivation was done to determine the tradeoff between the peak current (determined by the turn-on process) in $L_{\rm SN}$ and the ZVS range (during turn-off), using (31).

1) Turn-On Transitions: The Stage n°2 (see Section V-A) is divided into two subintervals according to the voltage across $\rm M_3$. Based on a balance of energies, the peak current $I_{\rm pk}$ is derived from

$$W_{\rm MAG}^{\rm pk} = \frac{L_{\rm SN}\cdot I_{\rm pk}^2}{2} = \frac{\frac{C_{\rm SN}\cdot V_{Bl}^2}{2}+\frac{C_{\min}\cdot(V_{Bl}-V_T)^2}{2}}{+\frac{C_{\max}\cdot\left(V_{Bl}^2-(V_{Bl}-V_T)^2\right)}{2}} \quad (32)$$

with $V_{Bl} = V_O - V_{\rm FC}$.

The upper switch transition is also implicated, the ZVS boundary condition is shown in

$$V_{\rm FC} \leq \sqrt{(V_{Bl}-V_T)^2+\frac{C_{\rm SN}+C_{\max}}{C_{\rm SN}+C_{\min}}\cdot\left(V_{Bl}^2-(V_{Bl}-V_T)^2\right)}. \quad (33)$$

2) Turn-Off Transitions: With the value of $C_{\rm SN}$ and the selected MOSFET (IPB65 R047 C7), the ratio $C_{\max}/C_{\rm SN}$ is around 7. The analytical formula (31) can then be applied with good accuracy. By using (32) and combining (23) with (31), a comparison of design constraints is given in Fig. 20 for a fast diode and SR. Assuming that ZVS is required from $\rm P_n$ to 50% of $\rm P_n$, values close to 4 and 6.8 μH are needed. In both cases, the peak current is lower than the nominal current (8.5 A).

An additional *RC* damping circuit placed across the snubber inductor will contribute to reducing the oscillations during transitions in Stage 4 during turn-on and turn-off and improve the CM emissions.

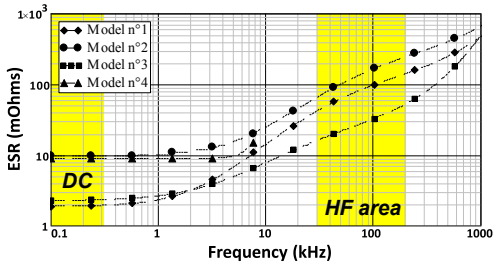

Fig. 21. ESR comparison of selected candidates to L_{SN}.

TABLE III
DESIGN CONSTRAINTS ON THE SNUBBER DIODES

	Rated voltage [V]	Peak current [A]
$\mathrm{D_{SN\,1}}$	V_O	I_I
$\mathrm{D_{SN\,2}}$	$V_O - V_{\mathrm{FC}}$	I_{pk} (from (32))

3) Design Recommendations: Due to the converter and snubber operations, the current through L_{SN} has a widely spread spectrum. Neglecting this property may lead to an inadequate design due to excessive skin, proximity, and core losses. A wise choice of L_{SN} and the *RC* damping circuit can reduce the high-frequencies stemming from the resonances and parasitic ringing. Hence, only the dc component and the first harmonics of F_{SW} are of interest. Even if custom designs remain possible (Litz wire, special winding arrangement), commercial inductors were preferred for cost reasons. Measurements were carried out with an impedance analyser (Wayne-Kerr 6500) to extract the ESR of selected models fulfilling the saturation requirements. The results of this measurement campaign are displayed in Fig. 21. Based on an estimation of losses and thermal constraints, Model n°3 (SER2900 Coilcraft) was selected.

D. Design of the Snubber Diodes

Table III summarizes the constraints over $\mathrm{D_{SN\,1}}$ and $\mathrm{D_{SN\,2}}$. Even if the turn-off transitions of the auxiliary diodes exhibit a low *dI/dt* due to L_{SN}, the mean and RMS current do not justify promoting the static characteristics. For this reason, high-speed-fast recovery diodes are preferred.

VIII. EXPERIMENTAL RESULTS

To demonstrate the effectiveness and the theoretical analysis of the proposed converter, a prototype was designed and tested. The electrical parameters of the converter are described in Table IV.

At the input side, there is a small HF DM capacitor (20-μF-film capacitor) to absorb the remaining part of HF current ripple and a dedicated *RC* network to stabilize the input voltage control loop. A CM filter was also implemented, not only to fix EMI issues but also to give a realistic industrial overview in terms of losses, volume, and mass of the overall converter. The dc-link capacitive bank was designed to absorb the 100-Hz fluctuating power with a peak to peak ripple of less than

TABLE IV
PARAMETERS OF THE PROTOTYPE

Power level	2000 W
Nominal input voltage V_I	234 V
Input voltage range	50–350 $\mathrm{V_{dc}}$
Maximum input current	8.5 A
Nominal output voltage V_O	330 V
Output voltage range	270–400 $\mathrm{V_{dc}}$
Switching frequency	30 kHz
Flying capacitors	$6 \times 1\mu$F SMD WIMA
DC-link capacitor	$5 \times 150\ \mu$F –450 V Electrolytic
Input DM inductor	KoolMμ ($\mu = 60$) +45 turns of AWG10
$\mathrm{M_1}$ and $\mathrm{M_3}$ if SR	IPB65 R047 C7
$\mathrm{M_2}$	IPB200 N25 N3
Freewheeling diode D	RUR1 S1560 S9 A
FC cell's diode	VS-15 ETH03 S
Snubber capacitor C_{SN}	2×1 nF/ ceramic C0 G
Snubber inductor	$4.7 - 6.8\ \mu$H if SR, SER2900 Coilcraft
Diodes $\mathrm{D_{SN\,1}}$ and $\mathrm{D_{SN\,2}}$	STTH3 R06

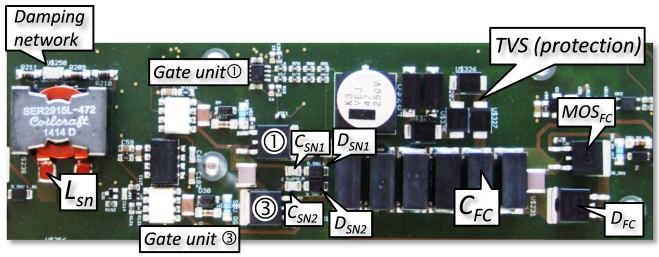

Fig. 22. Photograph of the semiconductors part equipped with the snubber.

10% under the worst-operating conditions (weak grid, i.e., $V_{\mathrm{AC}} = 160$ Vrms). Despite a relatively high-voltage ripple compared to conventional designs, very fast controls were implemented, in particular on the dc side to avoid degrading the MPPT efficiency [28]. All power devices were selected in D^2 Pak package, except the snubber diodes (SMB package).

A dedicated control loop was implemented for the FC to remain in the voltage range previously defined. A dynamically tuned PI compensator was chosen to avoid degrading the time response at light loads without compromising stability at full load. The impact of the snubber operations was taken into account by adding a feedforward term, derived from the analytical calculation.

The switching frequency was defined to maximize an efficiency/cost optimization function. A detailed analysis, taking into account an additional dc/ac stage, led to an optimal range of switching frequencies around 30 kHz. Below this value, the efficiency η is slightly increased as well as filtering devices related cost. Above, the cost remains stable but η is compromised.

A picture of the switching cells with a detailed view on the snubber part is shown in Fig. 22. Figs. 23–26 illustrate the waveforms of the proposed converter at full load and at the ZVS boundary with 234-V input voltage and SR. To justify that the operation remains unchanged even in case of voltage asymmetry between the main and the FC cells, measurements were performed with a *K* factor of 33% and 50% under nominal conditions (2 kW, 234 V, $D = 28.5\%$).

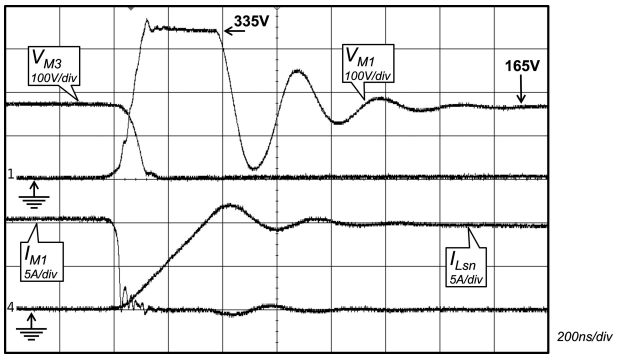

Fig. 23. Turn-off transitions (ZVS on M_1/ZCS on M_3).

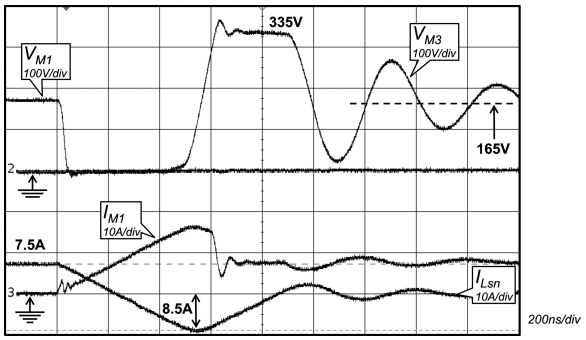

Fig. 24. Turn-on transitions (ZCS on M_1/ZVS on M_3).

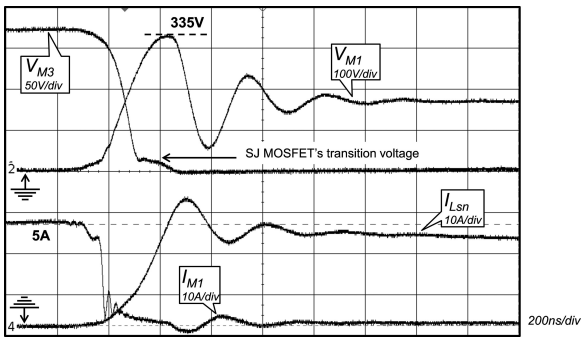

Fig. 25. Turn-off transitions at ZVS boundary on M_1

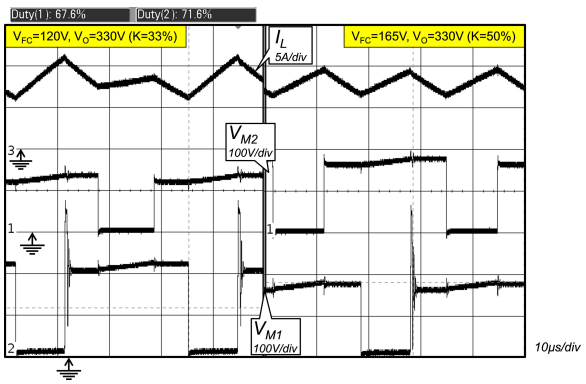

Fig. 26. Waveforms comparison for steady-state operations at nominal power with various value of the *K* factor.

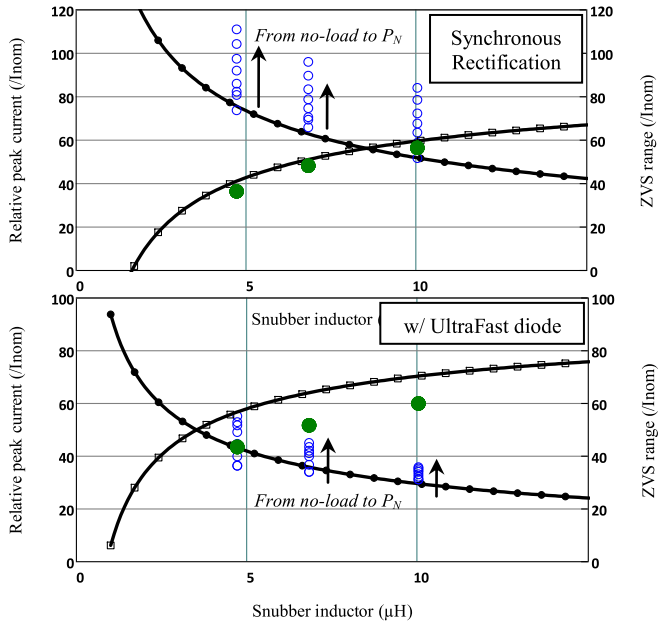

Fig. 27. Comparison between the proposed models and measurements. Peak current $I_{\rm PK}$: analytical (round markers), measurements (blue circles). ZVS range: analytical (square markers), measurements (green circles).

Fig. 26 shows the drain-to-source waveforms of M_1 and M_2 as well as the current in the filtering inductor. The ratio between current ripple, respectively, 5 and 3 A peak-to-peak fulfil the criteria of (5) and (6). With $K = 33\%$, the duty cycles have been measured with oscilloscope. The small difference between D_1 and D_2 of 5% justifies the choice of unique duty cycle in analyzing the circuit, as in Section III.

Experimental values of $I_{\rm pk}$ as well as the ZVS range were compared with analytical predictions, for $L_{\rm SN}$ =4.7, 6.8, and 10 μH. The results are displayed in Fig. 27.

For SR, the ZVS range is accurately predicted. Deviations exist on $I_{\rm PK}$, especially for increasing currents, attributed to recovery current, since for very light loads, measurements perfectly match the calculated values. This remark is confirmed by experimentation when the synchronous MOSFET is replaced by a freewheeling diode, the maximum deviation of the peak current being much smaller (bottom graph of Fig. 27). For the boost converter employing diode, the ZVS range is less accurately estimated and the peak current for small values of $L_{\rm SN}$ shows larger dispersion. This implies that a capacitive contribution has not been taken into account and as Fig. 19 suggests, even a small value of parasitic capacitance inevitably contributes to a non-negligible over sizing factor. *In situ* measurement identified an additional 320 pF to be coupled within the structure of the PCB.

In case of SR, the snubber inductor value of 4.7 μH ensures ZVS operations down to 900 W.

The conversion efficiency was then measured using a Yokogawa WT3000 precision power analyzer, having a power accuracy reading of $\pm 0.02\%$. The measured efficiency does not include the consumption of the auxiliary power. A fair comparison with a SiC diode (Cree C3 D10060) operating under hard-switching conditions was also considered to highlight the

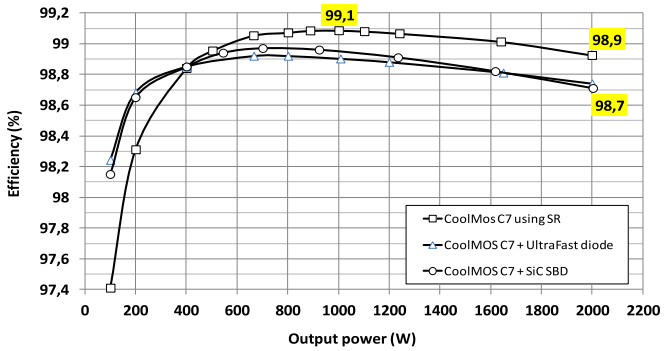

Fig. 28. Measured efficiency under nominal conditions at 30 kHz.

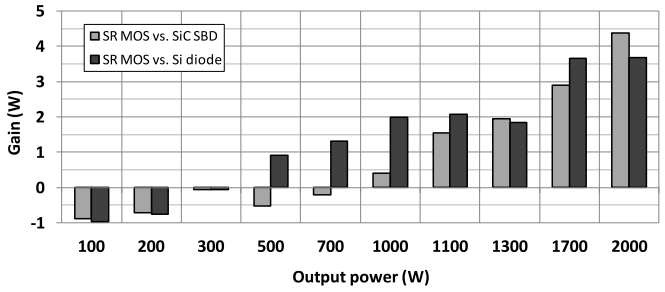

Fig. 29. Losses reduction under nominal conditions at 30 kHz.

impact of the snubber. Fig. 28 summarizes the efficiency curves. The loss reduction obtained with SR is given in Fig. 29.

From Figs. 28 and 29, it can be seen that the efficiency obtained with Si and SiC diodes are strictly identical. In particular, at light loads where conduction losses in the main devices are alleviated, the circulating energy in the snubber devices and partial ZVS conditions perfectly balance the switching losses of the SiC SBD-based solution. This is due to the fact that for very small currents, the voltage across the snubber is almost constant and equal $V_0 - V_{\rm FC}$. Since no recovery occurs due to ZCS transitions, the switching constraints between the two versions are exactly the same. The whole snubber costing around 2€, there is no direct performance/cost advantage in using either Si diode with snubber or SiC SBD only. However, implementing the Si-diode with snubber offers better EMI and improved component ruggedness. With SR, efficiency is improved by 0.2% at full load but slightly degraded at light loads. This effect directly stems from higher constraints imposed on the snubber—the peak resonant current being higher and the demagnetization stages longer due to additional parasitic capacitances $C_{\rm OSS}$. The conduction losses in the snubber diodes are then higher compared to the case involving a freewheeling diode. In the case of photovoltaic applications, this has no significant effect on European efficiency, and slightly favors the Californian efficiency.

Some additional advantages are applicable for the SR. First, the thermal management is made easier since the losses are reduced at the maximum power. Second, the present results are very promising for dc/ac structures for which MOSFETs are usually rejected due to the poor performances of their body diode. Considering the latest developments of SJ devices and the ever growing efforts made by manufacturers to optimize specific resistance while decreasing parasitic capacitances, such a simple and low-cost snubber appears adequate to compete with WBG devices (SiC or GaN) for tens-of-kilohertz applications.

IX. Conclusion

Based on a detailed analysis of a conventional three-level FC converter, an improved version is hereby proposed. It uses an asymmetric sharing of voltage constraints over the switching cells, enabling an optimal loss repartition between hard-switched low-voltage devices (250 V) and high-voltage devices (typically 600/650 V) assisted by a lossless snubber. ZVS/ZCS transitions are possible for both the switch and its freewheeling diode, eliminating the reverse-recovery effect and controlling the *dV/dt*. An extension to SR was also presented to further reduce the conduction losses of the freewheeling diode. Special attention was paid to include all parasitic elements of the devices, the highly nonlinear device output capacitance in particular, to avoid inaccuracies during the design process. The design of the proposed converter has been validated by experimental results from a 2.0-kW prototype. Experimental results confirm that the proposed structure can surpass a converter using SJ devices and SiC diodes at least up to 100 kHz. Finally, the 30-kHz prototype achieves an efficiency of $99\% \pm 0.1\%$ for load range $20 - 100\%$. A complementary experiment shows similar performance for a grid-tied inverter using the proposed conversion commutation leg.

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Guillaume Lefevre (M'14) was born in Bordeaux, France. He received the Graduate degree in electrical engineering from the Grenoble Institute of Technology, Grenoble, France, in 2001, and the Ph.D. degree from Joseph Fourier University, Grenoble, in 2004.

From 2004, he worked in different companies where he focused on power converters dedicated to sustainable energies and magnetic devices. Since 2011, he was a researcher in the Mitsubishi Electric R&D Centre Europe, France. His research interests include the analysis, design and optimisation of highly efficient converter topologies as well as soft switching techniques.

Stefan V. Mollov (S'98–A'00–M'03) received the Dipl.Eng. degree from the Technical University of Gabrovo, Gabrovo, Bulgaria, in 1995, and the Ph.D. degree from the University of Birmingham, Birmingham, U.K., in 2000.

From 2000, he was a Lecturer with the University of Birmingham, where his research activities focused on power electronics applications in the field of autonomous systems, aerospace electrical systems, and renewable energy sources and storage. In 2005, he joined ADETEL Group, France, as a Power Electronics Expert, working on transport applications. In 2009, he joined THALES Avionics as a Power Supply Expert. Since 2013, he has been the Head of the Power Electronic Systems Division at the Mitsubishi Electric R&D Centre Europe, Rennes, France.