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# Optimized Power Modules for Silicon Carbide MOSFET

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**Abstract**—an Integrated Power Board technology was used to construct a 3D power module. This packaging is suitable for use of WBG devices as it reduces the inductive parasitics to the strict minimum, with a 2nH loop inductance in our 1.2kV/80A SiC prototype using SiC MOSFETs. The packaging presents virtually no parasitics or necessity for slowing down the commutation, which is oscillation-free. The conducted emissions of the 3D module are more than halved in comparison to those of a bespoke wire-bonded, EMI-optimised module.

**Keywords**—Power module; 3D Packaging; SiC MOSFET; Wide band gap semiconductor, PCB, Embedded die.

## I. INTRODUCTION

The performance of Wide band gap (WBG) devices presents practical issues when replacing Silicon (Si) devices. It is clear that the better switching performances of WBG devices (higher switching speed and lower switching energy) can lead to a possible switching frequency increase and thus, a reduction in passive component volume [1][2][3]. However, the increase in transistor switching speed brings on higher influence of parasitic elements of device packaging. The most common problem concerns overvoltage across transistor caused by stray inductance of commutation loop. Packaging of power device is based on Direct Bond Ceramic (DBC) substrate and wire bonds. It is necessary to optimize it or to change of technology to realize packaging dedicated for WBG devices (i.e. with ultra-low parasitic elements). Therefore, only a dedicated packaging will permit to take the full advantages of WBG devices.

This paper focuses on Electro-Magnetic (EM) optimization of a power module dedicated on WBG devices – specifically, the clean switching behavior of the commutation cell. A state of the art of low inductance power module technology is shown in a first part and the EM design rules for power modules with WBG devices are thus reminded. Two power modules based on SiC MOSFET dies are presented: one, based on standard DBC substrate with wire bonds and the second, based on a 3D architecture realized using Printed Circuit Board (PCB) embedded die technology. Both modules then are compared in terms of electrical dynamic performance and Electro-Magnetic Interferences (EMI) behavior to confirm the clean switching behavior possible.

## II. STATE OF THE ART OF LOW INDUCTIVE POWER MODULES

Low inductive power module is an apparent trend in power electronic packaging. The first possibility to achieve a low

commutation loop inductance consists in optimizing layout of the DBC based power module. One example IGBT module has a low ampacity but is designed to easily parallelize several modules and thus to have a better current sharing between each module [4]. The commutation loop inductance is estimated to 10nH for one module with more than 50% of the value caused by module terminals. An optimized layout for SiC MOSFET 1200V 360A module is presented in [5], based on the parallelization of six commutation cells. However, the six commutation cells are placed following a geometry reducing electromagnetic flux of commutation loop and thus reducing the total stray inductance. Furthermore, a decoupling capacitor is connected to power module directly to the module terminals. With this design, the commutation loop inductance is estimated to 3.8nH and is achieved with classical fabrication techniques (DBC substrate, die soldering and wire bonds).

The replacement of wire bonds is also a major topic in packaging research. Indeed, this interconnection technology has several disadvantages: wire bonds lift off being one of the major causes of module failure, and the wire bonds are also great contributor to stray inductance, especially by the limitation they induced on power module layout. A possible solution to replacing wire bonds is to use a double face flexible PCB as interconnection between dies and DBC substrate [6]. The inverter leg is realized with 650V 600A IGBT and the double face flexible PCB allows new layout possibilities and thus commutation loop inductance reduction. EM simulation displays a commutation loop inductance of 16.25nH with the DC terminals claiming 14.85nH compared to the DBC substrate and flexible PCB claiming only 1.4nH. Furthermore, a similar solution is presented in [7] to realize a low inductive module for SiC MOSFET.

Three dimensional (3D) power modules are also an interesting solution to achieve a low dc loop inductance. This concept has been well studied for double side cooling systems where the power die is enclosed between two DBC substrates [8]. The electrical interconnection between power die top face and upper DBC is accomplished via copper posts, bumps or direct soldering [9]. An example high power density three phase inverter using a 3D power module with 1200V 15A IGBTs and 1200V 15A SiC Schottky diodes is shown to have an estimated loop inductance of 18nH [10]. In a more recent project [11], a 3D power module for SiC MOSFET is developed with a commutation loop of 7.5nH, shown in Fig. 1. The six commutation cells in this module are designed in a way as to allow magnetic flux cancellation.

As described in [12], realization of 3D module with DBC substrates follows a complex process. Soldering steps, DBC and chip alignments and electrical insulations are critical points which makes classical 3D module technology not ready for mass production. On the other hand, PCB process is a low cost/high volume process with 3D design capability. Embedding active or passive components inside PCB layers became a reality for low power electronic. An ultra-low inductive power module with SiC JFET using PCB process is presented in [13], where a JFET die is sintered on DBC substrate and a PCB circuit is realized on top of DBC substrate with an experimentally confirmed commutation loop inductance of 0.86nH. The PCB circuit copper tracks and the die are electrical connected with gold stud bumps. The electrical insulation is done by glass fiber reinforced epoxy (FR4), which is the classical dielectric material used for PCB realization. Furthermore, the structure permits to solder decoupling capacitors directly on top of power module, as shown in Fig. 2. Another example using a full PCB process has been developed for a 50kW three phase module using 650V IGBT chips for automotive applications [14]. Contrary to previous module, the chips are sintered directly on a 500 $\mu$ m copper lead-frame with the backside electrical insulation done with a dielectric layer compatible with PCB process. A cross section of the module is shown Fig. 3, and the experimental setup confirmed a commutation loop inductance of 2.8nH. Reliability and thermal management of PCB embedded die power modules have also been validated [15] [16].

### III. POWER MODULES FOR SiC MOSFET DEVICES

While it is clear that a low inductive commutation loop is necessary to achieve fast switching, it is also necessary to carefully design gate circuit for a clean gate control. Furthermore, Electro-Magnetic Compatibility (EMC) design rules can be also introduced at the basis of module design to avoid large EMI generation by the module itself. Thus, this section reviews the design aspects critical to module design for high switching speed capability. Afterwards, two SiC MOSFET power modules are presented with the same power dies and the same topology, i.e. inverter leg with decoupling capacitor, but manufactured with two different technologies: standard 2D DBC based process and 3D PCB embedded die technology.

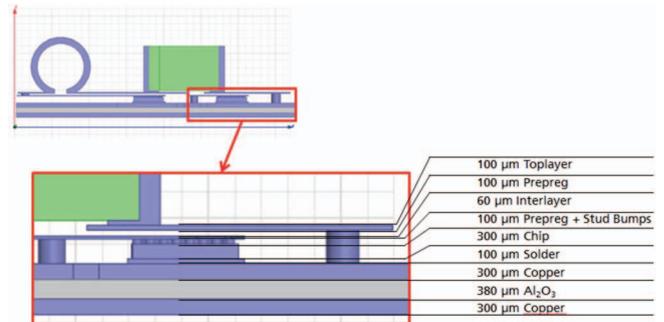
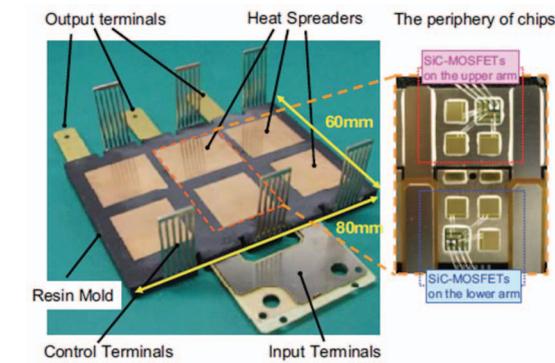


Fig. 2: Cross section of module developed in [13]

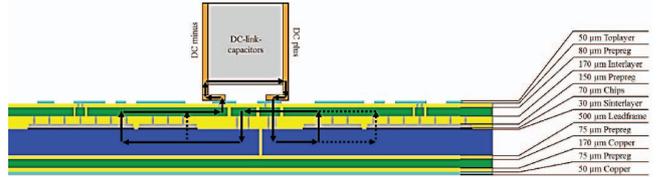


Fig. 3: Cross section of full PCB process module developed in [14]

#### A. Electrical design rules for high speed power transistor module

An electrical schematic of a commutation cell with two MOSFETs and associated parasitic elements, caused by the package, is shown in Fig. 4. The influence of each element critical to the electrical design is discussed via points 1) to 5).

##### 1) Commutation loop inductance

The commutation loop inductance is defined as the sum of the stray inductance ( $L_{s+}$  and  $L_{s-}$ ), the common source inductance ( $L_c$ ), the equivalent series inductance (ESL) of the decoupling capacitor ( $C_{dec}$ ) and mutual inductances between them. It is responsible of overvoltage during transistor switch off, which can lead to electrical breakdown. It also increases the switching energy by limiting the current slew rate. Hence, the commutation loop inductance must be minimized for good switching performance.

##### 2) Gate circuit inductance

The gate circuit inductance ( $L_g$ ) is responsible of gate-source over-voltage or sub-voltage leading to transistor gate oxide degradation. As gate circuit is equivalent to RLC series

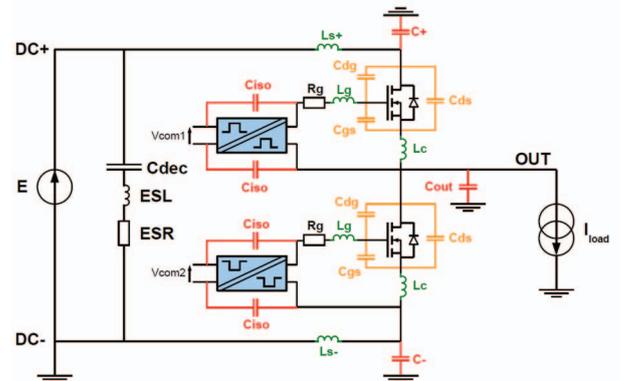


Fig. 4: Electrical schematic of commutation cell with parasitic elements

circuit (gate resistance  $R_g$ , gate inductance  $L_g$  and gate-source capacitance of transistor  $C_{gs}$ ), voltage overshoot is more pronounced with low  $C_{gs}$  value, which is the case for WBG transistor. Hence, the gate circuit inductance must be minimized for high reliability with fast switching devices.

### 3) Power/Gate circuit coupling

The power circuit can interact with gate circuit and create false turn-on phenomenon and two kinds of coupling exist: inductive and capacitive.

The inductive coupling is mostly caused by common source inductance ( $L_c$ ) where power current and gate current pass through the same conductor. The power current generates perturbations (over-voltage or sub-voltage) on gate circuit, and hence acts as negative feedback in the gate circuit, slowing down the current variation ( $di/dt$ ) during commutation and increasing the switching energy. Hence, the coupling between the power circuit and gate circuit must be minimized. The inductive coupling comes also from mutual inductance between power circuit and gate circuit (not shown in the schematic). The mutual inductance depends on gate circuit loop surface which receives magnetic flux generated by the power circuit loop. Hence, the gate loop surface must be decreased to minimize mutual coupling.

In terms of capacitive effects, the drain-source voltage variation ( $dv/dt$ ) generates parasitic current through the "Miller capacitance" ( $C_{dg}$ ) and can disturb the gate-source voltage until a false turn-on event occurs, as illustrated in Fig. 5. This problem is well known for high voltage IGBTs and a solution with "Active Miller Clamp" in gate driver IC's is well known. However, the problem is even more critical for WBG devices, where  $dv/dt$  is high and ratio between  $C_{dg}$  and  $C_{iss}$  ( $C_{dg}+C_{gs}$ ) rather small. Hence, the power module designer must avoid increasing  $C_{dg}$  capacitance with packaging layout. Furthermore, gate driver must be carefully designed in taking into account this phenomenon.

### 4) EMC issue

Due to the transition of voltages and current during switching, the commutation cell is necessarily a source of noise. The switching node (OUT) has a high  $dv/dt$  which creates common mode current through the common mode capacitor  $C_{out}$ . The parasitic capacitor of gate driver insulation ( $C_{iso}$ ) is also a path for common mode perturbations. Additionally, the parasitic capacitors  $C^+$  and  $C^-$  are linked to a stable potential ( $DC^+$  and  $DC^-$  respectively) and allow common mode current recycling inside the module. They can be considered as a part of the common mode filter. Note that

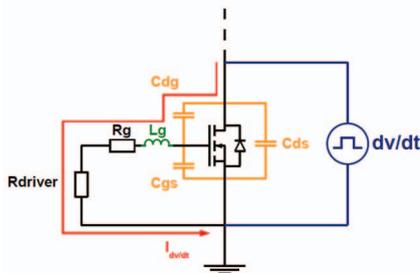


Fig. 5: Perturbation caused by "Miller capacitance" ( $C_{dg}$ ) and high  $dv/dt$

the DC bus voltage must be stable enough to avoid noise generation thanks to  $C^+$  and  $C^-$ . Hence, a reduction of common mode capacitance  $C_{out}$  is necessary. Finally, it is also important to have the  $DC^+$  and  $DC^-$  layout symmetric, and thus having same value for  $L_{s^+}$ ,  $L_{s^-}$  and  $C^+$ ,  $C^-$ , in the aim to avoid coupling between differential mode and common mode [17].

### 5) Die parallelization issue

Die parallelization is a common technique to increase the ampacity of power module. However, the layout must ensure that the power current is shared between dies, along with the gate current to each die. Thus, a symmetric layout for power track and gate circuit for each paralleled die is essential. Furthermore, symmetric layout allows respecting EMC issue as described previously.

### B. Power modules realization

Considering the electrical design aspects for high switching capability, two power modules with SiC MOSFET dies are presented to highlight the benefits of 3D packaging.

#### 1) Topology definition

The electrical schematic of power modules developed in this paper is shown in Fig. 6. The high side and low side switch are formed with four 1200V 80 m $\Omega$  20A SiC MOSFET dies from CREE (CPM2-1200-0080B) in parallel. For the sake of clarity, the gate and source connections of parallel dies are separated in Fig. 6 and the decoupling capacitor is considered part of the commutation cell. The Aresshield series 1kV 4.7nF ceramic capacitor in 0805 SMD package from KEMET is used because, for size constraint, it will be possible to use it in the both modules. Current sensors are not added to avoid increase size and parasitic elements of the commutation cell. The maximum working temperature of the selected capacitor is limited to 125°C. However, decoupling capacitor with 200°C maximum working temperature exists [18] and could be used in a future work.

#### 2) Module based on DBC substrate

The layout and module with standard DBC substrate and process are depicted in Fig. 7 and Fig. 8. The DBC substrate is made of 1mm thick AlN ceramic with 200 $\mu$ m copper layers and the top SiC MOSFET die interconnection is realized with 150 $\mu$ m Al wire bonds.

In order to reduce the commutation loop inductance, several techniques are considered. Firstly, the high side and low side dies are brought closer together and a decoupling

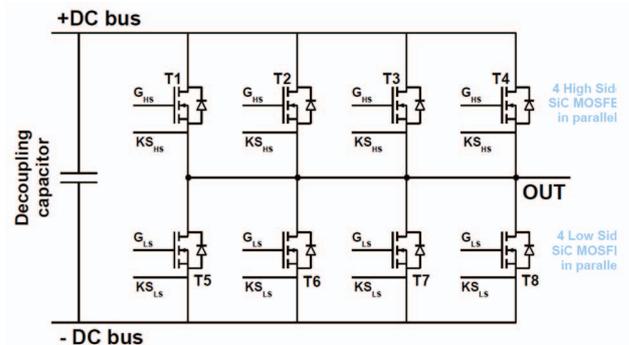


Fig. 6: Electrical schematic of power module realized in this paper

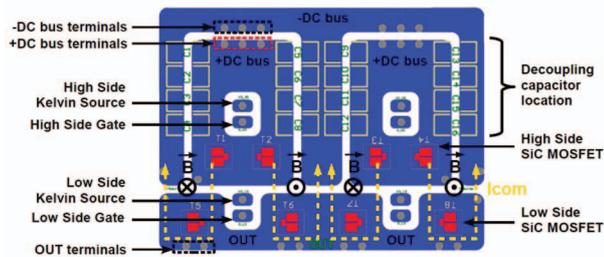


Fig. 7: Standard module layout



Fig. 8: Picture of standard module

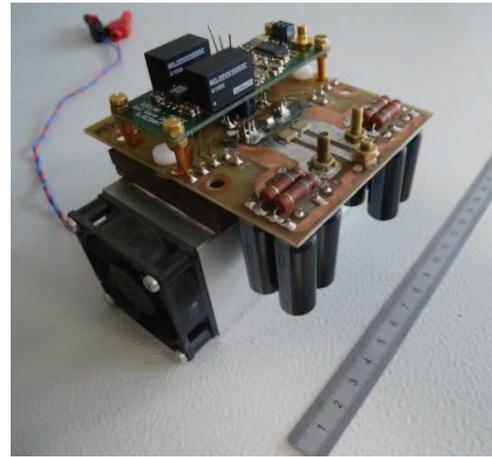


Fig. 9: Standard module assembly

capacitor is introduced inside the module. The commutation cell is thus limited to inside the module and the large inductance brought by the DC+ and DC- terminals are deported outside. Secondly, the four commutation cells are associated alternately in opposition from the commutation current point of view. As shown in Fig. 7, the commutation current ( $i_{com}$ , represented with yellow arrow) of each commutation cell generates a magnetic flux ( $B$ ) in opposition with neighbor cells and thus reducing the global stray inductance.

The coupling between power and gate circuits is attenuated with introduction of Kelvin Source (KS) connection. A dedicated wire bond brings the source potential to a kelvin source pin and the gate and kelvin source pins are situated close of each other as much as possible.

The module layout is made strictly symmetric between each commutation cells. The module is divided in two identical parts (two commutation cells in parallel for one part). The parallelization of the four commutation cells is realized via the PCB circuit on top of the module which allows soldering together pins with same electrical potential on a dedicated copper track. The final assembly is shown in Fig. 9 with forced air cooling system, interconnection PCB circuit and gate driver board.

In terms of the EMC issue, the output copper track area on DBC is reduced whereas +DC bus and -DC bus copper tracks area are equalized as much as possible. While a reduction of the output copper track area is critical for minimizing the cell commutation area, it is in contradiction with the current density requirement and thermal management. Hence, due to the 2D layout of DBC substrate, the optimization of electrical behavior and thermal management are in contradiction and thus, a compromise must be inevitably found.

### 3) PCB embedded die module

The layout capabilities offered by PCB process is used to realize an optimal 3D commutation cell. The schematic diagram of the proposed 3D module is shown in Fig. 10, with the basic concept being to include the commutation cell inside a bus bar. The high side and low side chip are superimposed one on each other, in a “Power Chip On Chip” (PCOC) concept [19] [20].

The realization of the power module is developed in the following points and begins by the fabrication of sub-modules (high side sub-module and low side sub-module):

- A layer of electrical insulated material (dielectric prepreg) is cut out at SiC MOSFET chip dimension and die is inserted.
- Laminate materials (prepreg and single thin copper layer) are laminated on each side of prepreg layer with embedded dies.
- Micro-vias on chip metallization (drain, source and gate) are done with laser drilling following by electroplated copper step. Micro-via diameter is  $150\mu\text{m}$  with pitch between two vias of  $250\mu\text{m}$  (ratio diameter/pitch of 0.6).
- A two layer PCB circuit is realized for gate circuit and laminated on source side of sub-module in fabrication. Electrical connection between layers is always done with copper filled micro-via process.

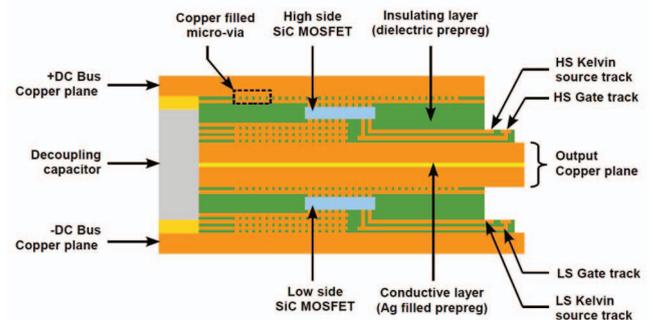


Fig. 10: 3D power module with embedded die technology

- Finally, the external thick copper plane (DC+ and Output for high side sub-module, Output and DC- for low side sub-module) are added by lamination and connected by micro-vias. The thickness of the layer is increased up to  $75\mu\text{m}$  due to the electroplated copper step which ensures flat surface.

At this stage, sub-modules are realized and the following process steps are required to make the final module:

- High side and low side sub-modules are laminated together with a conductive prepreg layer (Ag particles filled prepreg), ensuring an electrical connection for output copper plane of the both sub-modules.
- Ceramic SMD decoupling capacitors are soldered on module edge.

A picture of prototype is shown in Fig. 11. Dimensions of module, without taking into account the DC terminals, are  $30\text{mm} \times 30\text{mm}$  by  $2\text{mm}$  thick. The module embeds four SiC MOSFET dies in parallel for high side and low side switches. Twenty four decoupling capacitors (SMD 0805  $1\text{kV}$   $4.7\text{nF}$  Arcshield series from Kemet) are also soldered to the module edge, allowing perfect layout symmetry of each commutation cell (6 capacitors for each commutation cell). The final module with water cooling system and its associated electrical insulating layer (Blue layer) is shown in Fig. 12.

The bus bar concept of the module presents a low stray inductance, minimizing the commutation loop inductance. A symmetric layout is respected due to the decoupling capacitor

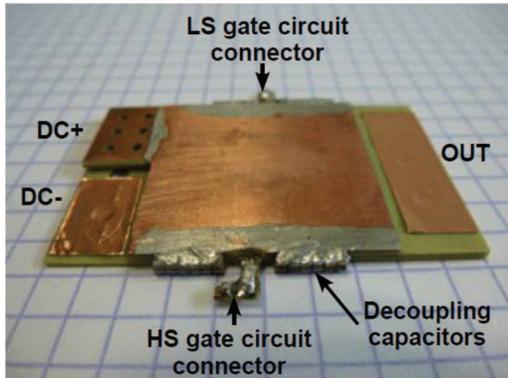


Fig. 11: Terminals definition of 3D module with embedded die technology terminals definitions

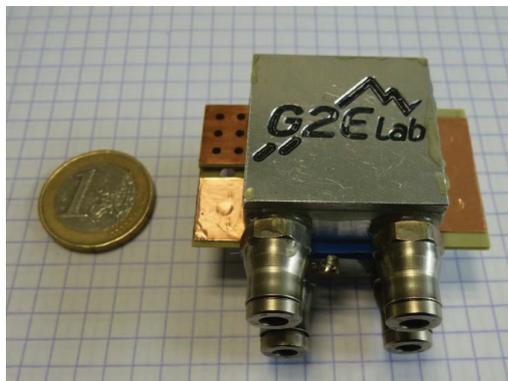


Fig. 12: 3D module with water cooling system

on the module edge. The gate circuit is realized with two superimposed layers inside the module. Thus, a small bus bar is realized allowing low gate inductance. The gate circuit is also symmetric to keep the gate signals synchronized. An additional gate-drain capacitor ( $C_{gd}$ ) is avoided by means of electrostatic shield of Kelvin source track (see Fig. 10). Furthermore, gate circuit geometry allows very low electromagnetic coupling between power and gate circuit because of a small gate loop area (only  $100\mu\text{m}$  spacing between gate and kelvin source track). However, the proposed structure increase inevitably drain-source capacitance ( $C_{ds}$ ) and gate-source capacitance ( $C_{gs}$ ) and using low dielectric permittivity prepreg is strongly required.

In terms of EMC issues, the switching node (Output copper plane) is placed in between the +DC bus and -DC bus, creating an electrostatic shield with the cooling system connected to earth. The common mode capacitor of the switching node is greatly reduced (theoretically nonexistent). Finally, the common mode capacitors referred to DC+ and DC- are increased due to the large surface with cooling system, which enables common mode current recycling inside the module.

In terms of the process, copper filled micro-vias replace wire bonds and soldering (or sintering) is therefore unnecessary for the die electrical connection. However, the proposed decoupling capacitor soldering on module edge is not an easy step and must be improved in a future work.

Finally, the module thermal management is more complex compared to standard power module. Indeed, cooling systems are required on each side of the module. However, the internal output copper plane acts as thermal drain (along with the dielectric prepreg), allowing heat to be spread on the whole surface inside the module. Thus, the cooling of each die could be qualified of  $2.5D$ , between single and double side cooling. Owing to the bus bar configuration, increasing the module surface is less critical for stray inductance and decreases significantly cooling system requirement. With PCOC module, the electrical and thermal issues are less coupled, as illustrated in [21].

#### IV. POWER MODULES DYNAMIC CHARACTERIZATION

##### A. Double pulse test configuration

The dynamic characterization of power modules is done with Double Pulse Test (DPT) fixture, as shown in Fig. 13. At first, a low voltage test with  $100\text{V}$  DC bus voltage and  $10\text{A}$

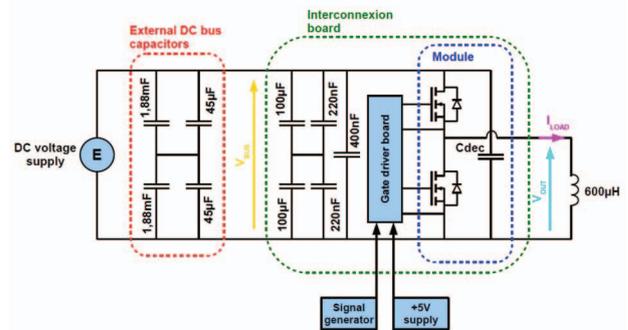


Fig. 13: Double pulse test bench

load current is realized with the aim to estimate the stray inductance. A high voltage test under 400V DC bus and 20A load current is then realized. In the low voltage test, the DC bus voltage ( $V_{bus}$ ) and the output voltage ( $V_{out}$ ) are measured with 300V 1GHz bandwidth voltage probe (Tektronix TPP1000). In the high voltage test, only the output voltage ( $V_{out}$ ) is measured with a 1kV 800MHz bandwidth voltage probe (Tektronix TPP0850). The load current ( $I_{load}$ ) is measured in both tests with 100MHz bandwidth current probe (TCPA300), with voltage and current waveforms being captured with a 2GHz bandwidth oscilloscope (Tektronix MSO5204). The same gate driver board is used for both modules and realizes gate-source voltage signal between +20V and -5V with external gate resistor of 2 $\Omega$ .

### B. Low voltage test

The low voltage test allows stray inductance estimation as a result of the oscillation on  $V_{out}$  just after low side switch turn-off, between the stray inductance ( $L_s$ ) and output capacitance ( $C_{oss}$ ) of the low side switch, as shown in Fig. 14. As the  $C_{oss}$  value is highly nonlinear with drain-source voltage, it is interesting to decrease DC bus voltage (100V in this test) in the aim to increase  $C_{oss}$  value to have higher oscillation level and lower oscillation frequency, allowing for easier determination of the stray inductance. Using the module datasheet, the  $C_{oss}$  of low side switch at 100V is estimated to be 732pF (4x183pF) for the standard module, and 883pF for the 3D embedded module – with the 3D architecture adding an additional 150pF.

Consequently, the results of DPT for standard module are shown in Fig. 15 and Fig. 16. Output voltage oscillations are about 130MHz leading to global stray inductance of 2nH. The results of DPT test for 3D module is shown in Fig. 17 and Fig. 18. However, contrary to standard module, no oscillations appear on  $V_{out}$  waveforms. For the 3D module, the stray inductance is so small that it cannot be estimated by the proposed method. However, as electrical configuration is identical to standard module (same SiC MOSFET dies, same gate driver board), it can be supposed stray inductance of 3D module is below 2nH.

### C. High voltage test

The high voltage test is done with 400V DC bus voltage and 20A load current with the output voltage waveform being of interest during the commutation event. The rising and falling transitions are shown in Fig. 19-Fig. 20 for standard module and in Fig. 21-Fig. 22 for 3D module. The rising time is equal to 14ns for both modules and falling time is equal to 30ns for both modules.

The high voltage test validates the electrical layout design

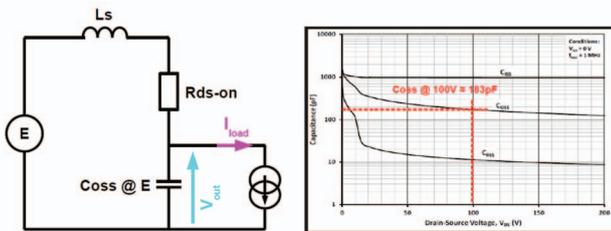


Fig. 14: Equivalent circuit for stray inductance estimation

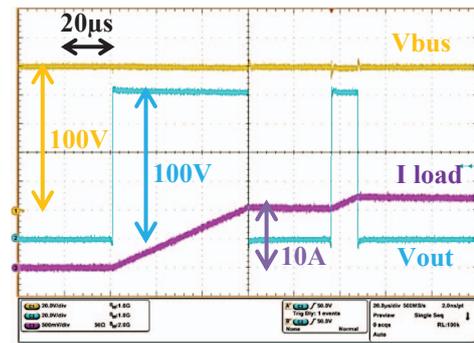


Fig. 15: General view of low voltage DPT for standard module

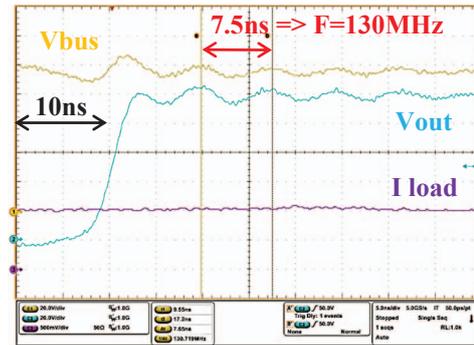


Fig. 16: Zoom on  $V_{out}$  during LS switch turn-off for standard module

for standard and 3D modules. A standard module with DBC substrate and wire bonds can be used for SiC MOSFET with an optimized layout design but the decoupling capacitor integration is the key point for this technology. However, with SiC MOSFET die improvement, new generations will inevitably switch even faster and hence, the 3D packaging with

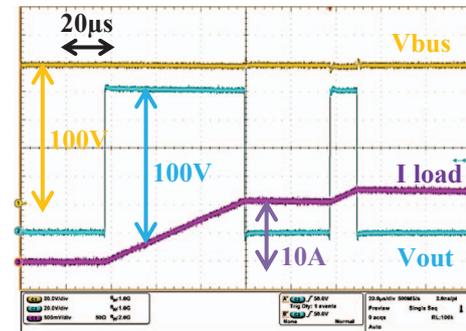


Fig. 17: General view of DPT for 3D module

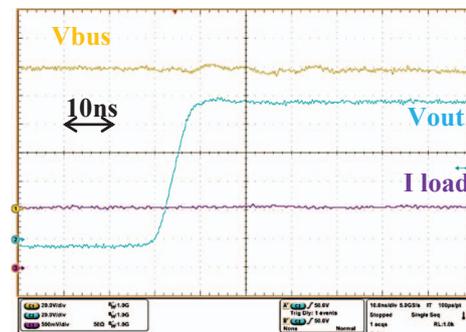


Fig. 18: Zoom on  $V_{out}$  during LS switch turn-off for 3D module

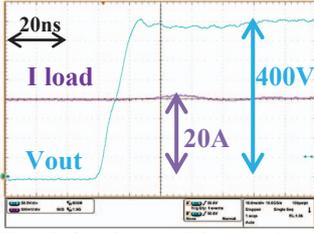


Fig. 19: Standard module Vout rise

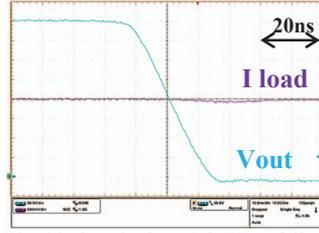


Fig. 20: Standard module Vout fall

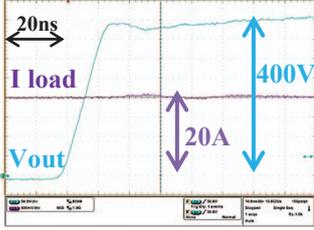


Fig. 21: 3D module Vout rise

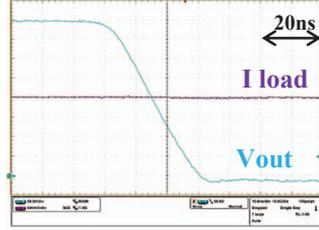


Fig. 22: 3D module Vout fall

embedded die technology offers more design capability. Moreover, electrical waveforms shown in this paper validate electrical behavior of this new packaging technology – especially considering the EMC behavior.

## V. POWER MODULES EMC COMPARISON

The two SiC MOSFET modules developed in this paper have been successfully tested in switching condition. The output voltage waveforms show high slew rate leading to likely high level of common mode current. Thus, the common mode current emission of each module is analyzed.

### A. Common mode capacitance calculation

The three common mode capacitances ( $C+$ ,  $C-$  and  $C_{out}$ ), described in Fig. 4, are calculated for each module with a planar capacitance formula. ( $C = \epsilon_0 \cdot \epsilon_r \cdot S / t$ ), and presented in Table 1. The standard module is made of high thickness (1mm) AlN DBC substrate, allowing low  $C_{out}$  value about 19pF. The standard module layout creates similar value for  $C+$  and  $C-$  around 30pF. In the case of 3D module,  $C_{out}$  value is theoretically zero (electrostatic shield). Furthermore,  $C+$  and  $C-$  values are quite large (239pF) and identical because the whole surface of upper and lower side of the module (30mm x 30mm), in front of the two water cooling system, is concerned.

Hence, as the 3D module has the advantage of extremely low  $C_{out}$  capacitance, and simultaneously, increased  $C+$  and  $C-$  capacitance for better common mode current filtering. A high dielectric constant insulating material could also be used to increase even more  $C+$  and  $C-$  value, which is absolutely impossible for standard module.

### B. Test bench presentation

The theoretical advantage of proposed 3D module is tested with EMC test bench (Fig. 23) and both modules are compared in terms of common mode (CM) voltage amplitude in conducted mode (i.e. from 150 kHz to 30 MHz). The test is done without load to suppress influence of load parasitic elements. A DC Line Impedance Stabilization Network (LISN) is inserted between 400V DC supply and device under test. The

Parameters	Standard module	3D module
Dielectric type	AlN	SILPAD 1500ST
Dielectric thickness $t$ (mm)	1	0.203
Dielectric constant $\epsilon_r$ (@ 1MHz)	9	6.1
$C+$ surface $S$ (mm <sup>2</sup> )	400.5	900
$C+$ capacitance value (pF)	31.9	239
$C-$ surface $S$ (mm <sup>2</sup> )	329	900
$C-$ capacitance value (pF)	26.2	239
$C_{out}$ surface $S$ (mm <sup>2</sup> )	239.5	0
$C_{out}$ capacitance value (pF)	19.1	0

Table 1: Common mode capacitance value of standard and 3D modules

switching frequency is set to 70 kHz and the modules are tested with their associated cooling system connected to earth.

### C. Common mode voltage spectrum comparison

The envelope of CM voltage for the 2D (blue curve) and the 3D (red curve) module, between 150 kHz and 30 MHz, is shown in Fig. 24. The CM voltage amplitude of the 3D module is lower compared to 2D module with reduction between 6dB $\mu$ V (for first concerned harmonic at 210 kHz), until more than 15dB $\mu$ V at 12MHz. Note that a 6dB $\mu$ V reduction corresponds to two times less emissions.

Fundamentally, the advantage of the 3D module based on PCOC concept is experimentally validated for CM noise reduction. The standard module developed in this paper is highly optimized and EMC comparison with industrial module will certainly show a more significant difference. In a future paper, it will be necessary to include a representative load in EMC tests, as it is possible the load CM impedance influences more CM spectrum than the module itself.

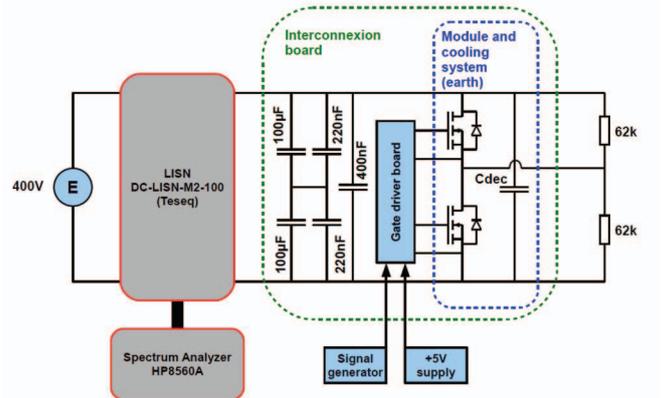


Fig. 23: EMC test bench

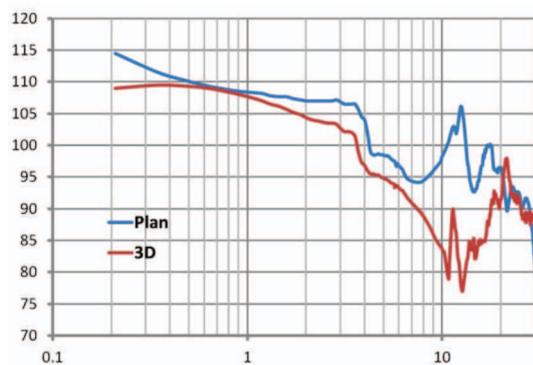


Fig. 24: Common mode voltage spectrum comparison

## VI. CONCLUSIONS AND PERSPECTIVES

The dedicated packaging for WBG devices is an apparent need for efficient power converters to properly exploit the potential switching characteristics offered by WBG devices. In this paper, the electrical design rules for high speed transistor module have been reviewed and applied to realize two SiC MOSFET modules: one with classical DBC substrate and wire bonds technology and another with PCB embedded die technology. The dynamic characterization show clean switching events for both modules without overvoltage or oscillations. The stray inductance is estimated to 2nH for standard module and certainly less for the 3D module (too small for estimation). It is confirmed that a low inductive power module with DBC substrate and wire bonds can be realized by carefully designing the module layout but the 3D design capability of PCB embedded die technology gives more degrees of freedom for commutation cell parasitic elements optimization. Moreover, the 3D architecture based on PCOC concept, allows for a common mode noise reduction which has been validated with experimental test bench.

While the thermal and reliability issues have not been treated in this paper, an optimal power module design must be done in taking into account both electrical and thermal aspects. With the 3D module architecture presented in this paper, the both constraints are less coupled. Furthermore, in terms of reliability, PCB embedded die technology seems to be very promising considering the removal of the wire bond interconnections. In the future, with increasing WBG device performance, 3D package appear to be interesting due to their ability to reduce the commutation cell parasitic element and the PCB embedded die process is a promising technology to realize this 3D packaging. Finally, to go further in power module integration, the embedding of gate driver IC's and decoupling capacitor is the next consideration.

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