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***Abstract*—A new three dimensional package based on Printed Circuit Board (PCB) embedded die technology is presented in this paper. The package takes advantage of the Power Chip On Chip (PCOC) concept, where commutation cell is housed within the bus bar, allowing a very low inductance design for the package of up to 0.25 nH. Two key design challenges with the package relate to the layout and the thermal management. Thus, a parallelization technique enabling impedance balancing is developed for the layout and validated using four parallel Silicon Carbide (SiC) MOSFETs. Gate circuit is carefully designed allowing low inductive behavior and low electromagnetic coupling. Finally, the thermal management of the module is studied and die attach with direct copper filled vias is validated.**

Keywords—3D packaging, Power Chip On Chip, Embedded die, SiC MOSFET, Paralelling.

I. INTRODUCTION

Over the past decade, Wide Band Gap (WBG) semiconductors have seen an increasing presence, not only in research, but also emerging commercial applications. Their improved switching characteristics and lower on-state resistance allow for a potential increase in converter power density due to decreased cooling or filter effort. However, owing to the large stray inductance of traditional packaging techniques, the improvement in switching speed has yet to be fully realized. Thus, much effort has been dedicated to improving this traditional two-dimensional package, with the state-of-the-art allowing for a reduction in commutation loop inductance below 1 nH [1] [2] [3] [4]. In addition, owing to the fast voltage/current transitions desired from the package the Electro-Magnetic Compatibility is also an issue. Therefore, the common mode capacitance must be similarly minimized to enable fast voltage transitions.

In this paper, the Power Chip on Chip (PCOC) is employed to achieve a lower inductive path and a reduction in common mode capacitance. The principle of the PCOC concept (Fig. 1) and a first realization was achieved with a press-pack solution [5]. Furthermore, a second realization (Fig. 2) of this same concept has also been illustrated with Direct Bond Copper (DBC) substrates and in PCB [6]. Using the PCOC concept, a PBC-based package with embedded power dies and a novel die attach is the focus of this work.

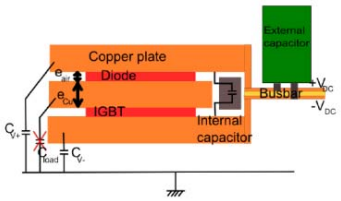

Fig. 1: The PCOC electrical concept; switching cell integrated in the busbar [5]

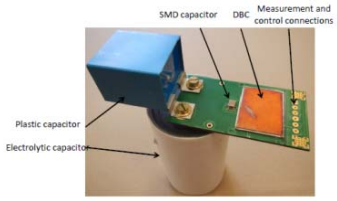

Fig. 2: PCOC module with DBC and PCB realization [6]

The targeted application for the concept package is a high-density 25kVA, 75 kHz three-phase inverter with 800V DC bus voltage. Due to the limitations in current SiC MOSFET die sizes, paralleling dies is necessary to achieve the rated power for the module. However, current balancing between each die is not obvious, and owing to the intended switching speed of the module, a critical issue for the robust application of the package [7]. Furthermore, due to the proposed embedded PCB process, the thermal layout is also a critical point to achieve the high power density expected from this package. Therefore, this paper focuses on two key points critical for the realization of this package: the electrical characterization, to ensure balanced currents and the appropriate number of SiC dies, as well as the thermal design for reliable operation.

II. PCOC MODULE WITH PCB EMBEDDED DIE PROCESS

The proposed PCB based PCOC package embeds a power die into a dielectric layer (the prepreg layer), and with copper filled vias, electrically connect the die to the copper layers needed for power flow. Each of these layers is added by a lamination process, similar to the process illustrated in the HI-LEVEL project [8]. In this paper, contrary to previous project, copper filled vias are used for the die attach, instead of sintering or soldering step. Specifically, the Drain, Source and

Gate pads of a SiC MOSFET are connected to its environment with vias filled of copper by electrolytic deposition with the die metallization suited for the copper growth step. A 200nm chromium hang layer is deposed on die pads followed by 1-2µm copper layer. An overview of the proposed PCOC module with embedded die is shown in Fig. 3. The half bridge module is divided in two quasi-identical sub-modules, one for the high side switch and one for the low side switch, which are finally laminated together with appropriate electrically and thermally conductive prepreg.

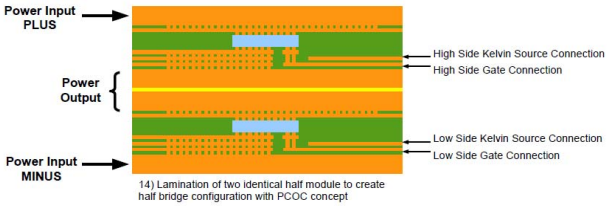

Fig. 3: PCOC module with embedded die overview

Layouts of the two sub-modules are shown in Fig. 4 and Fig. 5. The electrical connections with external circuits are done by extension of copper layers and the power inputs DC+ and DC- are connected to an external bus bar. The gate circuits are then connected to external gate driver.

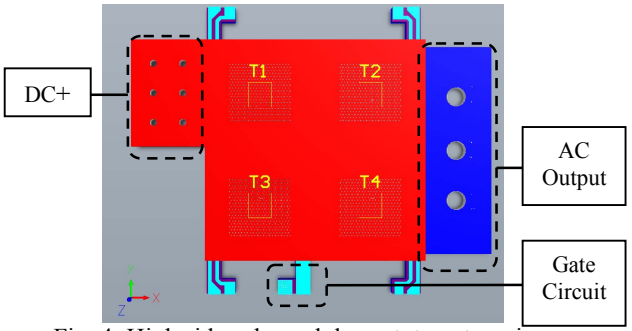

Fig. 4: High side sub-module prototype top view

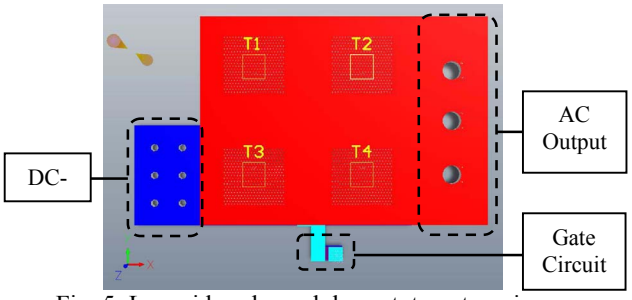

Fig. 5: Low side sub-module prototype top view

III. Optimal Number of Die in Parallel

The proposed packaging is designed assuming 25kVA output power, a DC bus voltage of 800V with a switching frequency of 75 kHz and SiC MOSFET dies CPM2-1200-0080B from CREE (the datasheet and the SPICE model of the die was used for switching energy estimation). Therefore, assuming these conditions, the appropriate numbers of dies were selected and the current balancing issues can be highlighted.

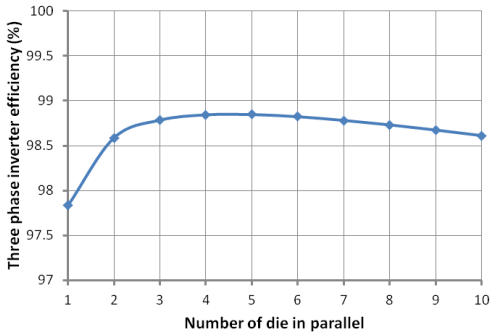

Fig. 6: Three phase inverter efficiency in function of number of die in parallel

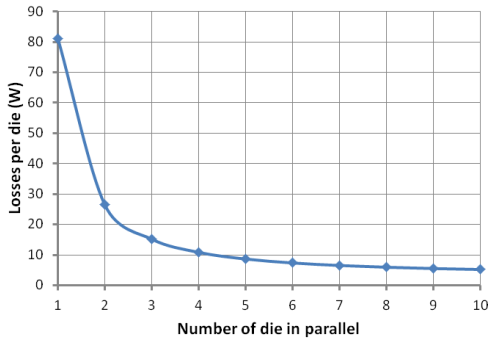

Fig. 7: Loss per die in function of number of die in parallel

Using the loss characteristics of the SiC MOSFET, the influence of the parallelization of the dies is shown in Fig. 6 and Fig. 7, with a peak inverter efficiency of approximately 98.8% achieved with four parallel dies. Another advantage of parallelization is to reduce loss density by distributing the losses over a larger area. The selected SiC dies have a surface about 11mm² which leads to power density of 227W/cm² for two dies in parallel and falling down to 91W/cm² for four dies in parallel. Thus, the losses are better distributed and the number of potential hotspots in the module is reduced.

IV. Electromagnetic Design

The proposed module's inductive parasitic elements are modeled using the Partial Element Equivalent Circuit (PEEC) simulation tool (INCA3D). The module is composed of four parallel dies in half bridge configuration (8 at all), resulting in a square shaped module with power input (DC+ and DC-) on left side and power output on right side (AC), as shown in Fig. 8. The gate circuits for high side dies and low side dies are realized with a gate track superimposed on Kelvin source track. Furthermore, the module dimension and geometry are chosen in order to minimize the commutation loop inductance, the gate circuit inductance and limit power/gate interactions between power and gate circuitries.

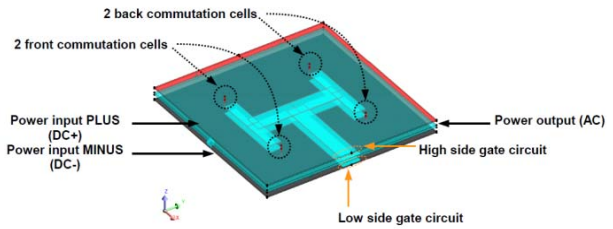

Fig. 8: PEEC simulation of PCOC module with four parallel commutation cells

The module dimensions are fixed to 30mm x 30mm and a total thickness of 2mm. Assuming decoupling capacitor as close as possible to the input face DC+ and DC-, the two front commutation cells have a commutation loop inductance about 0.7 nH, whereas the two back commutation cells have a commutation loop inductance about 1.5 nH. Thus, the power commutation path is clearly unbalanced, which leads to a dynamic current unbalance during switching transition.

A. Commutation loop: impedance balancing issue

In order to avoid the dynamic current unbalance, a decoupling capacitor is soldered on module edge to improve the symmetry of the commutation loop in each commutation cell. Due to the low thickness of the module (2mm), a small SMD capacitor is chosen (Kemet Arcshield 1kV 4.7nF SMD 0805). The equivalent capacitive characteristics have been measured with an impedance analyzer (Agilent 4294A), resulting ESR of 92.6mΩ and an ESL of 226pH. Six capacitors are placed in parallel on each commutation cell, leading to 24 capacitors in parallel on the module edge. An explode view of module PEEC model with decoupling capacitor is shown in Fig. 9. An equivalent circuit for the six decoupling capacitor of each commutation cell is connected to the module edge between DC+ and DC-.

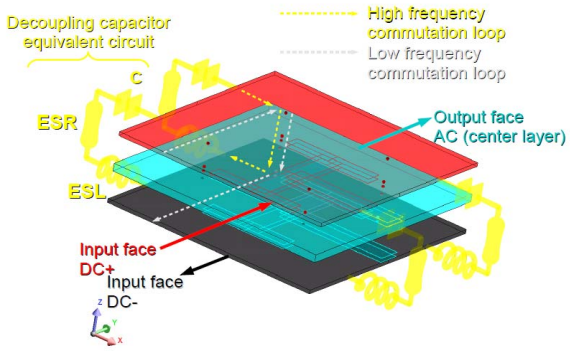

Fig. 9: PEEC simulation of PCOC module with four parallel commutation cells and decoupling capacitor on module edge

The power loop impedance of the front and back commutation cells were then simulated and the result is shown in Fig. 10. In a first state, for frequency up to 10 MHz, impedances are unbalanced which corresponds to an inductive value of 1.5 nH for front loop and 0.7 nH for back loop. A resonant phase between decoupling capacitor and commutation loop inductance appears in a second state from 10 MHz to 80 MHz and is shown in state "2" in Fig. 10. The third state begins above a frequency of 80 MHz where decoupling capacitor act as short circuits and modify the commutation loop inductance value, which is approximately 0.25 nH for the both loops. In order to balance the dynamic current, the equivalent frequency of current in switching transition must be high enough to fall in this range. The SiC MOSFET selected in this project offers current rising time around 3ns corresponding to an equivalent frequency of 110 MHz (f_{eq}=0.35/T_{rise}), or region "3" highlighted in Fig. 10.

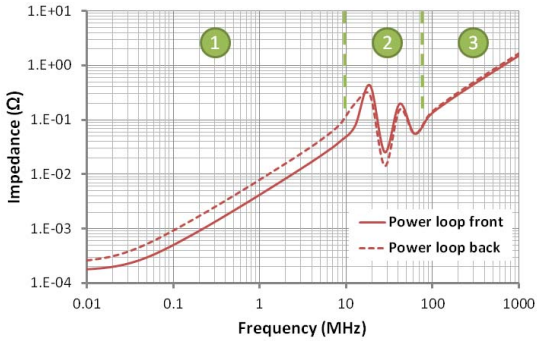

Fig. 10: front and back power loop impedance simulation with decoupling capacitor on module edge

In order to validate the simulation, a mock prototype was built (Fig. 11) with a 30mm x 30mm by 2mm thick PCB with 105µm copper plane on external faces and 16 decoupling capacitors on the module edge. To model the commutation cell in a switching state during the impedance measurement, a short circuit was realized between plus and minus terminals from the vias located on the unpopulated die positions in the front loop and back loops. The measurement connectors are located on the two free edges such that the front commutation loop and back commutation lopp impedance can be measured by simply reversing the mock prototype. The mock prototype impedance measurement presented in Fig. 12 confirms the same behavior as the simulation, with impedance balancing in high frequency range (above 60MHz). Power loop inductance is estimated at 0.23nH for the front loop and 0.21nH for the back loop – indicating a much better path inductance match for better dynamic current balancing.

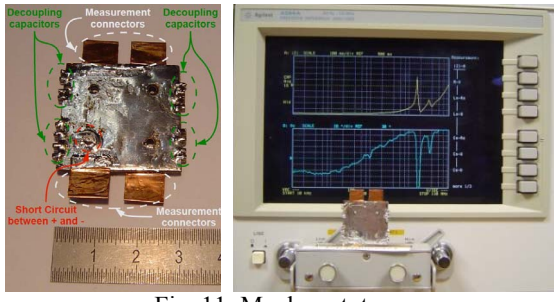

Fig. 11: Mock prototype

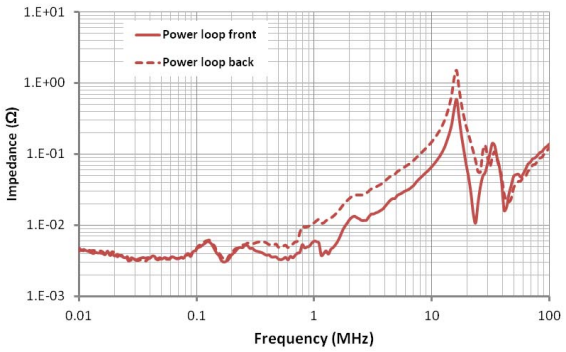

Fig. 12: Front and back loop impedance measurement on mock prototype

B. *Gate circuit*

The gate circuit is a crucial part for any WBG device module. The parasitic elements, especially the inductance, can create unacceptable overvoltage leading to gate destruction. Hence, the electromagnetic coupling between power loop and gate loop is a critical design issue to maintain reliable operation of the module. Furthermore, in the case of parallel switching devices, the balance between gate signals is also critical to the design. Therefore, a gate circuit layout is proposed in this PCB-based module resulting in a low inductance, low coupling and perfect balancing between parallel dies. The gate circuit layout and associated INCA3D model is shown in Fig. 13.

The gate circuit is composed of two superimposed tracks: one for the gate and one for the kelvin source track.. A kelvin source is connected as close as possible to the source of each MOSFET die allowing a good decoupling between the power and the gate circuitries. Two layers of each half module are dedicated to the layout of the gate circuit. The superposition of the both tracks realizes a small busbar leading to very small gate inductance. As the gate inductance value depends on geometry parameters such as track width, track length and spacing between gate and kelvin source layers, a PCB process offers very good performance due to the small spacing until 50µm.

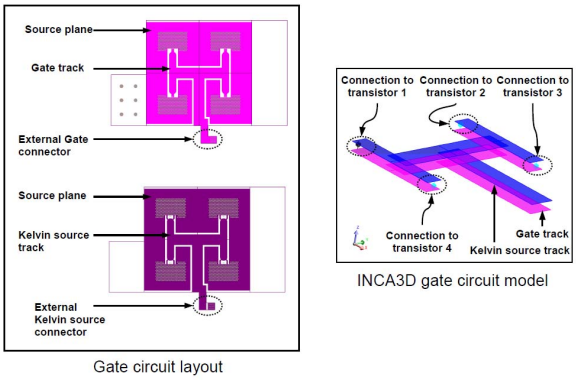

Fig. 13: Gate circuit layout and associated INCA3D model

1) Gate circuit inductance: influence of track width and spacing

The influence of track width and spacing is studied using INCA3D. A small bus bar is realized with one centimeter length and 35µm copper thickness as depicted in Fig. 14. Track width is varying between 0.5mm and 4mm and the spacing between the two tracks is set to 100µm, 75µm and 50µm, with the resulting inductance shown in Fig. 15.

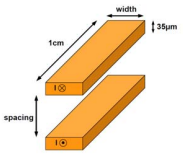

Fig. 14: Busbar geometrical parameters

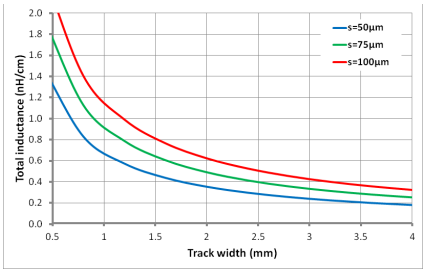

Fig. 15: Busbar inductance in function of track width and spacing

Increasing track width from 0.5mm to 2mm allows for a decrease in the inductance of about 70% for all selected spacing, with the gain being less significant for the larger track. Furthermore, decreasing track spacing of 25µm allows inductance reduction about 25%. In the both cases, the reduction in inductance is caused by mutual inductance increase. As space constraints are not significant in this layout, the track width has been selected between 2mm and 3mm. Thus, spacing is a less significant parameter and 100µm spacing has been selected. The circuit, as shown in Fig. 13, is simulated and the gate circuit impedance is calculated in function of frequency, as shown in Fig. 16. The gate circuit inductance is deduced from this result, which is equal to 1.3nH. Thus, even if gate circuit is long (approximately 30mm), by optimizing the spacing and by using a strip line approach, the gate inductance can be greatly reduced

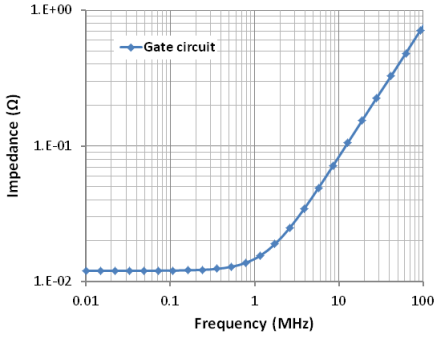

Fig. 16: Gate circuit impedance

2) Electromagnetic coupling estimation

The goal of this section is to study interaction between power loop and gate loop. The most significant problem comes from the common inductance between gate and power loop. Using a kelvin source connection allows to suppress it. Indeed, the two loops are well separated. Thus, coupling between the both loops comes only from mutual inductance, Mgs, as seen in Fig. 17.

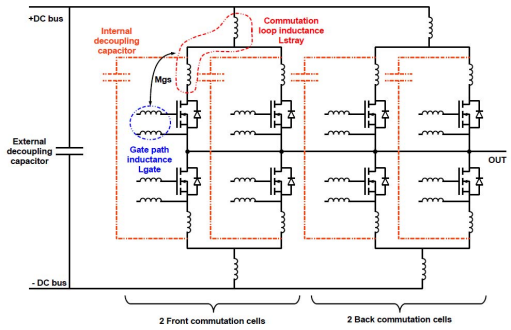

Fig. 17: Parasitic inductance and mutual inductance in the module

The mutual inductance is defined by geometrical parameters, which especially includes the common surface of the both loop. In this design, the gate loop is interlocked inside the power loop; the surface of the gate loop is the interesting parameter for the mutual inductance minimization. As gate and kelvin source tracks are superimposed one on each other with 100µm spacing, surface of the gate loop is significantly reduced and depends only on the track length, thereby resulting in a small mutual inductance value.

To quantify the coupling between the both circuits, the coupling coefficient is introduced (1). This coefficient is varying between 0 (no electromagnetic coupling) and 1 (perfect electromagnetic coupling). In the case of transformer, coupling coefficient must be as closed as possible to 1. Hence, the coupling coefficient must be closed to 0. Simulations are realized with simultaneous calculation of power loop and gate loop of each die. One simulation is done with short circuit on a front die and another one with short circuit on back die. Simulations are done in high frequency (300MHz). Results are shown in Table 1.

$$K_{gs} = \frac{M_{gs}}{\sqrt{L_g \cdot L_s}} \quad (1)$$

Table 1: Coupling coefficient simulation results

Gate circuit	**Kgs (p.u.)**	
	Front loop	*Back loop*
G1	0.0114	0.0170
G2	0.0028	0.0160
G3	0.0013	0.0003
G4	0.0020	0.0025

Via Table. 1, the coupling coefficient is always less than 0.02. Electromagnetic coupling is thus extremely small, power and gate circuit can be considered uncoupled.

V. Thermal Analysis

The thermal management is a design challenge for the PCOC module, since two dies are located on top of each other due to density constraints. Furthermore, the intended die attach employs copper filled vias, which increases the thermal complexity. Therefore, the design of these vias is developed firstly using an equivalent thermal conductivity. In a second part, the 3D geometry of PCOC module is simulated to examine the influence of the prepreg thermal conductivity and the external copper layer thickness.

A. Equivalent thermal conductivity for die attach vias

In the embedded die process, each chip is connected to the copper planes using filled copper vias, which must be designed to ensure low thermal resistance. Several design parameters can be modified to decrease thermal resistance such as pitch, diameter, pre-preg thermal conductivity, and area. Experimental performance of thermal via and equivalent model is proposed in [9] [10] [11]. To simplify the design process, an equivalent thermal conductivity of via region based on 1D thermal resistance is used, as shown in Eq. 4. This equivalence is validated by FEM simulation and shows error on temperature distribution less than 4%.

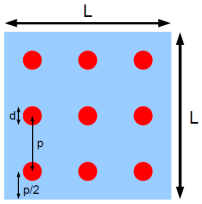

Fig. 18: Via region geometrical parameters definition

$$S_{region} = L^2 = N_{via} \cdot p^2 \quad (2)$$

$$Rth_{region} = \frac{e}{S_{region} \cdot \lambda_{preg}\left[1 + \frac{S_{via}}{S_{region}}\left(\frac{\lambda_{cu}}{\lambda_{preg}} - 1\right)\right]} \quad (3)$$

$$\lambda_{eq} = \lambda_{preg}\left[1 + \frac{\pi}{4}\frac{d_{via}^2}{p^2}\left(\frac{\lambda_{cu}}{\lambda_{preg}} - 1\right)\right] \quad (4)$$

Eq. 1: Via region equivalent thermal conductivity

The equivalent thermal conductivity of via region as a function of diameter on pitch ratio (d/p) is depicted in Fig. 19, assuming a thermal conductivity of copper equal to 380W/m.K and two values of prepreg thermal conductivity: 0.25 W/m.K for classical prepreg and 3W/m.K for advanced prepreg.

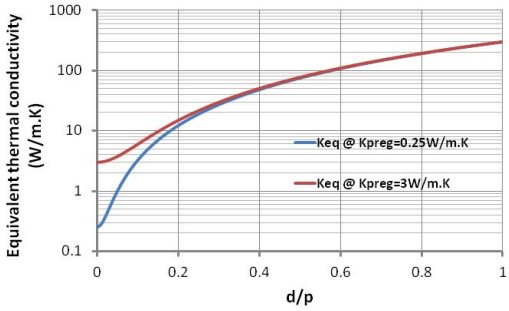

Fig. 19: equivalent thermal conductivity in function of d/p ratio

Accordingly, the equivalent thermal conductivity is largely influenced by d/p ratio. With respect to the prepreg, the thermal conductivity does not influence the overall thermal conductivity if the d/p ratio is greater than 0.3. Therefore, it is possible to use a classical prepreg without degradation in terms of thermal performance. In terms of comparison, the state of the art in die attach, i.e. Ag nanoparticles sintering, offers thermal conductivity of 240W/m.K and the classical die attach with Au80Sn20 eutectic alloy has thermal conductivity about 58W/m.K [12]. Thus, with considerations of the design rules imposed by the PCB manufacturer, the die attach can be designed with a significant improvement on classical die attach methods, i.e. 100 W/m.K using a d/p ratio of 0.6.

B. Pre-preg and external copper thickness

The PCOC module has a complex 3D geometry and therefore simplifications are necessary to efficiently simulate this package with FEM software. The thermal exchange on module edge is negligible and thus adiabatic boundary condition is considered. Due to the symmetry of the four commutation cells, only one cell is taken into account. A die is therefore considered as 3mm x 3mm, with only a quarter of the structure represented. Identical cooling system is necessary on the both side of the module and PCOC module presents a quasi-symmetry with the central layer (AC output), thus only one half module is considered (identical high side or low side module). The resulting simulated FEM model is shown in Fig. 20, with die losses of 10W, a via diameter on pitch ratio of 0.6 (corresponding to PCB manufacturer design rules) and an external temperature equal to 50°C.

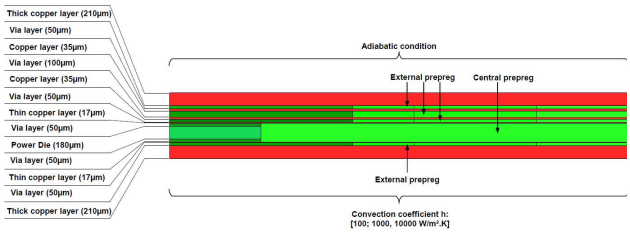

Fig. 20: PCOC module geometry for thermal simulation

Using the simulation model, the central prepreg is identified as another possible path for thermal flux. In varying its thermal conductivity from 0.25W/m.K to 3W/m.K, die temperature decrease is limited to 3K, assuming 210µm thick copper and h=1000W/m.K. This effect is even less pronounced as the copper thickness increases.

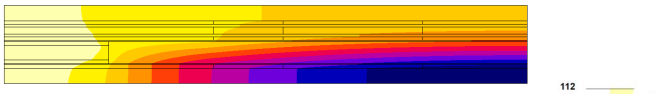

Fig. 21: PCOC module thermal simulation with central prepreg thermal conductivity of 0.25W/m.K

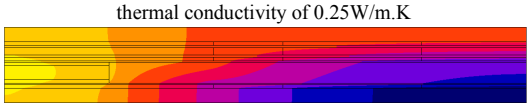

Fig. 22: PCOC module thermal simulation with central prepreg thermal conductivity of 3W/m.K

Due to its role in the thermal loading of the package, the influence of external copper thickness is examined for various convection coefficients and with a central prepreg thermal conductivity of 0.25W/m.K. Temperature distribution along exchange surface is illustrated for three convection coefficients (100W/m².K, 1000W/m².K, 10000W/m².K), as shown in Fig. 23-25.

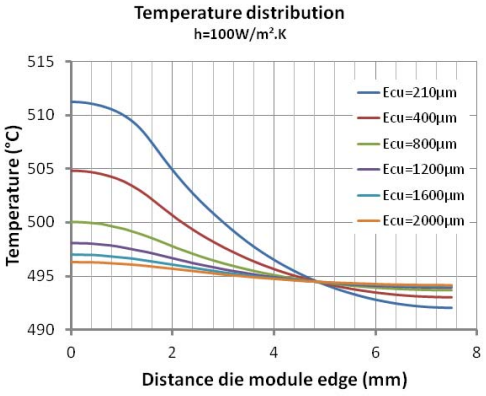

Fig. 23: Copper thickness influence, h=100W/m².K

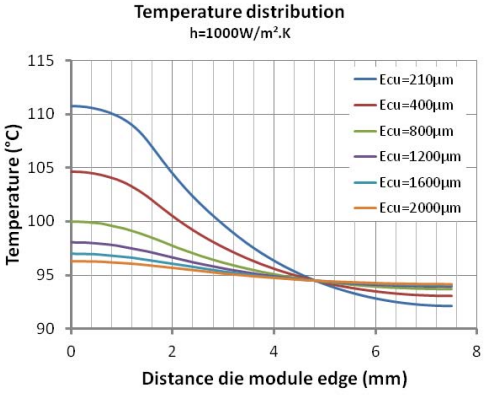

Fig. 24: Copper thickness influence, h=1000W/m².K

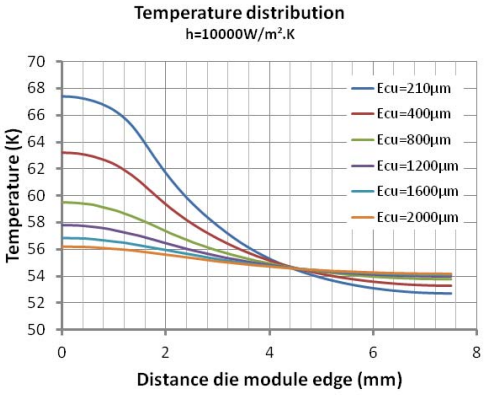

Fig. 25: Copper thickness influence, h=10000W/m².K

As can be observed from Fig. 23-25, the external copper plane thickness has a significant impact on the thermal management. Ideally, a thickness of 1.5mm would suite the application but the standard PCB process limits the value of this copper thickness. Therefore, in the considered prototype, a thickness of 210µm has been chosen due to process limitations on the first technical realization. Note that for die working temperature below 125°C with 210µm copper thickness, it is determined that the equivalent convective coefficient of cooling system must be greater than 800W/m².K.

VI. Conclusion and perspectives

The PCOC module with embedded die technology enables the realization of a compact, high density power module. The concept enables a very low inductive design, making it suitable for wide band gap device application with fast turn on and turn off times. In this paper, electromagnetic design is developed. A solution for the dynamic current sharing between parallel dies has been presented and validated. The stray inductance of the package is estimated around 0.25nH. Gate circuit has been optimized and simulations shows low inductive behavior and low electromagnetic coupling with power loop. The thermal simulation confirms the thermal stability of the package. However, PCB manufacturing process limitations are shown to constrain the copper thickness, which plays a key role in the thermal management.

In a future work, the prototype developed in this project will be characterized in an electrical and thermal point of view. Reliability of assembly is also a key point. The module is built in a symmetric way allowing compensating the thermo-mechanical stress caused by CTE mismatch between materials. Thermo-mechanical simulation and active power cycling must be realized to validate the concept.

High temperature package for WBG device is an actual trend. An operating temperature of 225°C could be imagined with assembly proposed in this paper by replacing standard prepreg with polyimide which has glass transition temperature about 250°C. However, tradeoff is necessary between losses increase in WBG device caused by higher junction temperature and gain in terms of cooling system reduction.

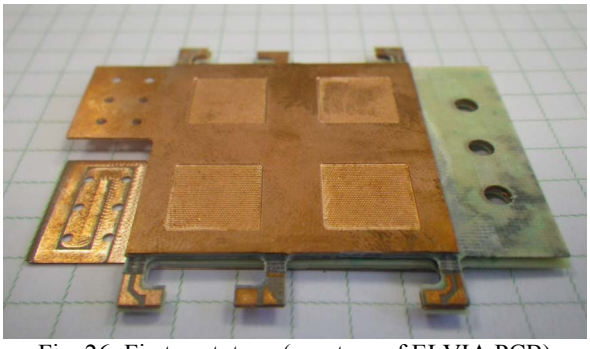

Fig. 26: First prototype (courtesy of ELVIA PCB)

References

[1] J. N. Calata, J. G. Bai, X. Liu, S. Wen and G.-Q. Lu, "Three-Dimensional Packaging for Power Semiconductor Devices and Modules," *IEEE Transactions on Advanced packaging,* vol. 28, no. 3, p. 404, 2005.

[2] L. Ménager, C. Martin, B. Allard and V. Bley, "Industrial and lab-scale power module technologies: A review," in *IEEE 32nd Annual Conference on Industrial electronics, IECON*, 2006.

[3] E. Hoene, A. Ostmann, B. Lai, C. Marczok, A. Müsing and J. Kolar, "Ultra-Low-Inductance Power Module for Fast Switching Semiconductors," in *PCIM Europe Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy management*, 2013.

[4] E. Hoene, A. Ostmann and C. Marczok, "packaging Very Fast Switching Semiconductors," in *International Conference on Integrated Power Electronics Systems (CIPS)*, 2014.

[5] E. Vagnon, P.-O. Jeannin, J.-C. Crébier and Y. Avenas, "A Bus-Bar-like Power Module Based on Three-Dimensional Power-Chip-on-Chip Hybrid Integration," *IEEE Transactions on industry applications,* vol. 46, no. 5, p. 2046, 2010.

[6] J. Marchesini, P. Jeannin, Y. Avenas, L. d. Oliveira, C. Buttay and R. Riva, "Realization and characterization of an IGBT Module based on the power Chip-on-Chip 3D Concept," in *energy Conversion Congress and exposition (ECCE)*, 2014.

[7] C. Martin, J. Schanen, J. Guichon and R. Pasterczyk, "Analysis of Electromagnetic Coupling and Current Distribution Inside a Power Module," *IEEE Transactions on Industry Applications,* vol. 43, no. 4, p. 893, 2007.

[8] C. Neeb, J. Teichrib, R. D. Doncker, L. Boettcher and A. Ostmann, "A 50kW IGBT Power Module for Automotive Applications with extremely Low Dc-link Inductance," in *Power Electronics and Applications (EPE'14-ECCE Europe)*, 2014.

[9] D. Gautam, D. Wager, F. Musavi, M. Edington, W. Eberle, W.G. Dunfold, "A review of Thermal Management in Power Converters with Thermal Vias", in *Applied Power Electronics Conference and Exposition (APEC),* 2013.

[10] R.S. Li, "Optimization of Thermal Via Design Parameters Based on an Analytical Thermal Resistance model", in *Thermal and Thermomechanical Phenomena in Electronic Systems (ITHERM'98)*, 1998.

[11] S. Lee, T.F. Lemczyk, M.M. Yovanovich, "Analysis of Thermal Vias in High Density Interconnect Technology", in *Semiconductor Thermal Measurement and management Symposium (SEMI-THERM VIII)*, 1992.

[12] V. Manikam and K. Cheong, "Die Attach Materials for High Temperature Applications: A Review," *IEEE Transactions on Components, Packaging and Manufacturing Technology,* vol. 1, no. 4, p. 457, 2011.