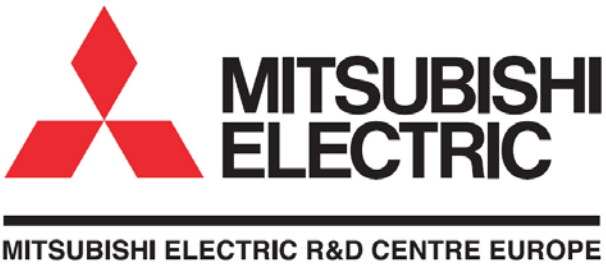

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Multi-objective optimisation of a bidirectional single-phase grid connected AC/DC converter (PFC) with two different modulation principles

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Multi-objective Optimisation of a Bidirectional Single-Phase Grid Connected AC/DC Converter (PFC) with Two Different Modulation Principles

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***Abstract*—A design methodology is presented for a full-bridge Power Factor Corrector (PFC) converter with two control schemes: the well-known Continuous Current Mode (C.C.M) and Triangular Current Mode (T.C.M). The second one is an extension of the Discontinuous Current Mode (D.C.M). The converter is composed of one high frequency leg and one leg switching at the grid frequency and includes the EMC (common and differential mode) filter. This work highlights the impact of the modulation scheme on the design of passive components and on the overall losses. A pareto front in the efficiency (η) *vs* power density (ρ) domain is derived for both modulation schemes and for natural convection cooling. We show that, when EMC issues are considered, the T.C.M poses more constraints for partial load operation, superseding the full-load design. Finally, it is shown that for non-interleaved converters C.C.M modulation is better than T.C.M modulation, resulting in higher density converters.**

***Index Terms*—Optimisation procedure, pareto front, PFC, modulation, wide band-gap devices.**

I. Introduction

POWER converters are commonly used in grid connected applications such as electrical vehicle on-board battery charger [1] or solar application [2]. Power factor correctors (PFC) are frequently used to ensure an almost sinusoidal grid current in order to comply with harmonic standards. The usual constraints for power converters are high efficiency, high power density and reliability. Table I presents performances of some high density power converters, with different features. These examples use wide band-gap devices, e.g., Silicon Carbide (SiC) or Gallium Nitride (GaN) or new generation Super Junction devices (SJ Si). The development of wide band-gap devices allows an increase in switching frequency, leading to a reduction of the overall volume [5].

Table I: Example of high density converters

References	Efficiency[%]	Power Density [kW/L]	Features
[1]	95 %	5 kW/L	uni. / iso.
[2]	97.2 %	4.3 kW/L	bidirectional
[3]	95.4 %	8.72 kW/L	bidirectional
[4]	96.4 %	8.18 kW/L	bidirectional

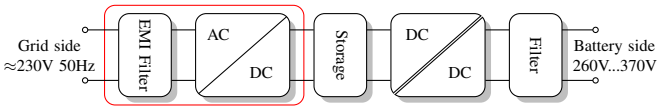


Figure 1: Functional bloc representation of the 3.3kW converter, the red box corresponds to the part discussed in this paper.

The work presented in this paper is a part of a project which aims to design a highly integrated, isolated and bidirectional 3.3kW converter. The chosen application for this proof of concept is an on-board battery charger for an electric vehicle. Figure 1 is a representation of the global converter to identify the different functions implemented in the project. The converter presented in this paper corresponds to the PFC part including the differential mode (DM) and common mode (CM) filters. The main specifications of the 3.3 kW PFC are listed in Table II on page .

The objective of this work is to design a converter which corresponds to the best trade-off between efficiency and power density using pareto front analysis. This method is commonly used in power electronics to optimise power converters [6], [7] and magnetic components [8], [9]. This kind of optimisation allows an easy analysis of the impact of different variables used in the design procedure. In this case, the final trade-off is defined according to efficiency and power density. The chosen topology for the PFC is a full bridge boost topology composed of one "high frequency leg" (Q1, Q3) and one

Table II: Specifications of the 3.3kW AC/DC Converter

RMS Input Voltage Range (AC)	85-260 V
RMS Maximal Input Current (AC)	15 A
Maximal Output Current (DC)	12 A
Output Voltage (DC)	400 V
Maximal Output Power	3.3 kW
Working Environment	-40 to 60°C
E.M.C	EN55011 Class B conducted EMI

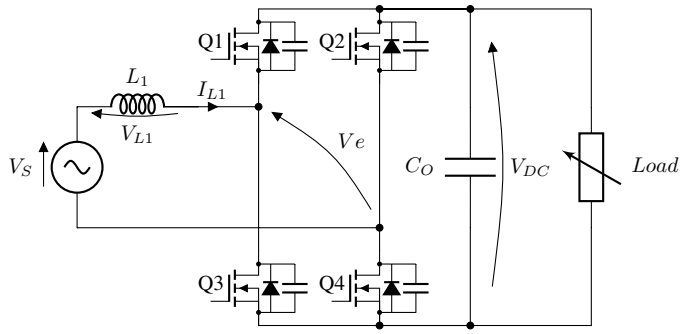


Figure 2: PFC Full-Bridge Topology, Semiconductor devices are represented with their body diode and parasitic output capacitor. Q1 and Q3 operate at high frequency whereas Q2 and Q4 operate at the grid frequency.

leg switching at the grid frequency (Q2, Q4) as illustrated in Figure 2 on page . This topology allows to reduce the requirements on the boost inductor value [10]. Several control schemes are possible for this topology and two are considered here. The first one corresponds to C.C.M which is quite classic and the second one to T.C.M which recently gained interest after the the Google little box challenge [4]. In spite of a certain number of papers dealing with T.C.M [11], [12] there are only very few comparisons between the two modulation principles. A comparison is provided in [4] where the T.C.M is presented as slightly less performant. This paper proposes a design procedure to confirm and explain the lower performances of T.C.M for a different application which is a 3.3 kW bidirectional PFC with natural convection.

This paper is composed of four main parts; the global methodology and common points used for optimal design for both modulation schemes are presented first. The second and third parts are dedicated to C.C.M and T.C.M respectively. The waveforms are widely different according to the modulation which to highlights how the modulation impacts the design. Then, the last part corresponds to the comparison of the two converter designs.

II. Design Procedure

This section presents the design flow used to determine the best trade-off between efficiency and power density for the converter in Figure 2 on page and its EMI filter. This design procedure is presented in Figure 3 on page for both modulation schemes. The flowchart is composed of three main parts: “semiconductor”, “EMI filter design” and “Inductor”. These three parts are thereafter presented in more details. First of all, important waveforms are determined analytically for a set of variables depending on the modulation. These variables are presented respectively in parts III and IV. Waveforms (inductor current and switch voltages and currents) are used in the design to identify the most suitable devices, to optimize the passives and to design the EMI filter. The sub-part on EMI filter design considers multistage filters, the number of stages being an additional variable independent of the input parameters. The outputs of each parts are losses and volume which are used to select the final converter.

At the end of the procedure, the impact of the thermal management on the global power density is added. Natural convection is assumed in this work. A preliminary study was carried out according to specification to determine the volume of the heat sink as a function of global losses. It was found a thermal coefficient of 5cm^3/W is a sensible value according to the specifications: ambient temperature of 60°C, and the maximum devices temperature of 125°C.

A. Inductor design

The design of the inductors, e.g., boost inductor or input filter inductor, is a key point in the optimal design. In this work, the well known technology of planar inductor design is selected due to its acceptable level of integration [13]. Global inductor losses are composed of copper losses and core losses. Copper losses are generated by the current flowing through the PCB traces and are influenced by skin and proximity effects. The current is composed of low and high frequency harmonics. The resistance seen by each harmonic is different due to these effects. An equivalent AC resistance (R_{AC}) is determined with 3D FEM simulations. For core losses, the improved generalised Steinmetz equation (iGSE) method is used [14]. This method decomposes the inductor current in major and minor loops. Major loops correspond to the induction created by the low frequency component (50 Hz) whereas the minor loops correspond to the induction generated by the high frequency components (f_{SW}). More details are presented in [13].

B. EMI filter design

The EMI filter design includes inner optimisation loops. Regarding the CM filter, CM currents are calculated based on approximated parasitic capacitors and duration of commutations (which depends of the selected semiconductor and also ZVS commutation). The chokes are designed using a database for standard nanocrystalline cores. This type of material presents a high permeability which allows to reach high inductor values with a reduced number of turns. Common mode capacitors are selected in a database of Y2 ceramic capacitors. The following presents with more details the design procedure of the DM filter. To focus on integration, multistage filters are considered. It was shown in [15], that the lowest volume of multistage filters is obtained for identical cells, though the volume sensitivity is negligible. In this work, each stage includes same inductors but different capacitors. This involves a slight increase of the volume but allows spreading the resonant frequencies and a decrease in capacitor current density in the first stage. The elementary cell corresponds to a second order LC filter with a parallel R-Cd damping circuit. The number of stages (elementary cell) is variable in our design procedure. The DM filter design allows compliance with EN55011 class B standard, the model used in the design procedure is presented in Figure 4 on page . The first step for DM filter design is the calculation of the required attenuation. FFT is used to obtain the spectrum of the voltage across R3, which is a 50 Ω resistor. This spectrum is then compared with EN55011 class B average standard. The required attenuation

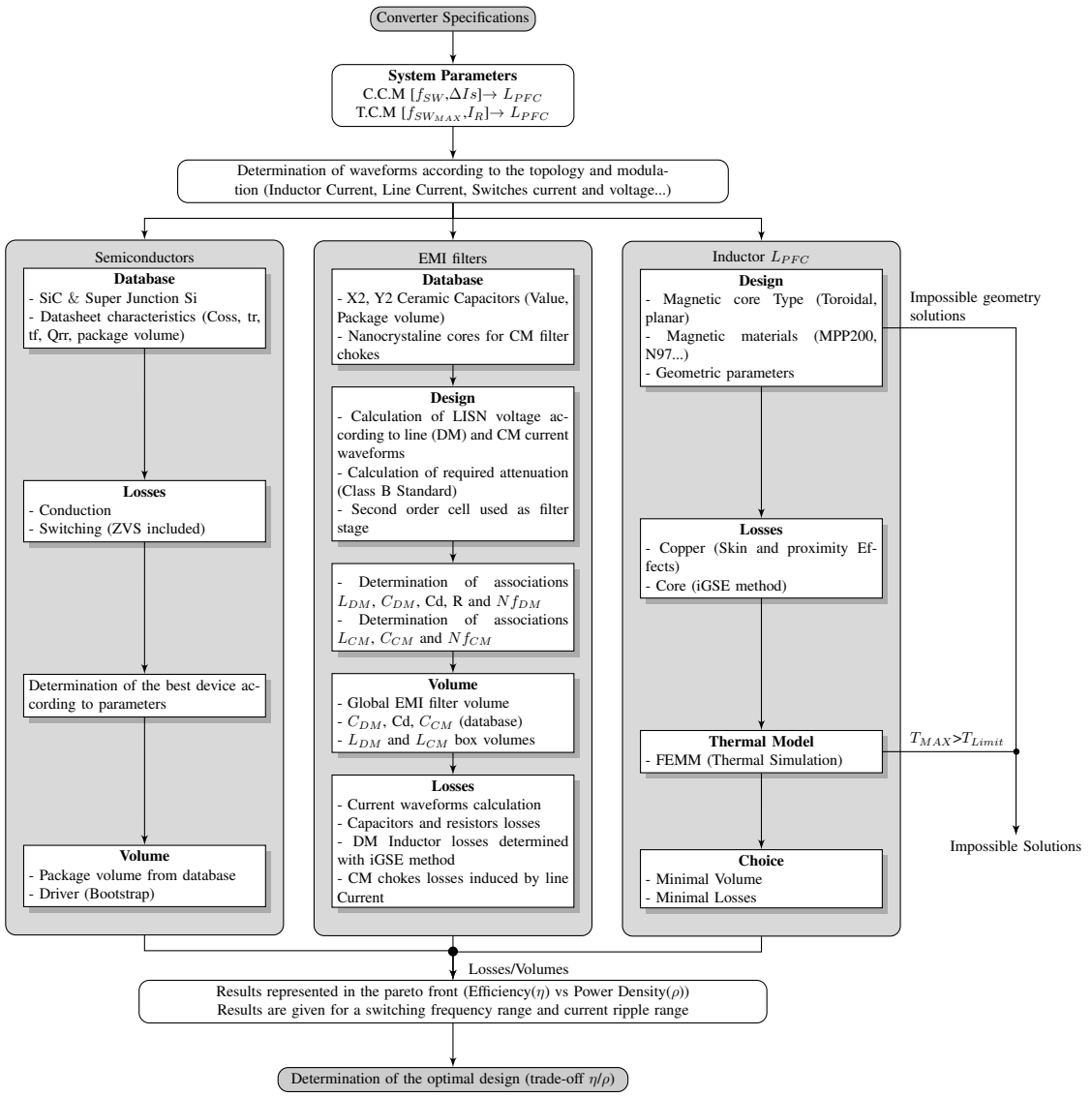


Figure 3: Design Flow Chart presents the optimization procedure which involves several inner optimizations as inductor, semiconductors and EMI filters

and the dimensioning frequency (F_D) are determined by (1) with a margin set to 6 dB.

$$Att_{req}(F_D) = max(FFT(V_{R3}) - Standard + Margin) \quad (1)$$

The second step corresponds to the determination of the DM capacitors, which depends on the number of filter stages. For this design, a database of X2 ceramic capacitors was created. Ceramic capacitors are preferred to film capacitors due to their higher density. First, a global capacitance is calculated to achieve a certain power factor. The damping capacitors (C_D) are also included in the global capacitance. For that criteria we use the case corresponding to minimal load, which is 10% of the full load, P_{MIN}= 330 W. The minimal selected power factor is cos φ = 0.995 at this power, giving a maximum reactive power of Q_{MAX} = 33 VAr. The allowable global capacitance of the DM filter is then calculated using equation (2).

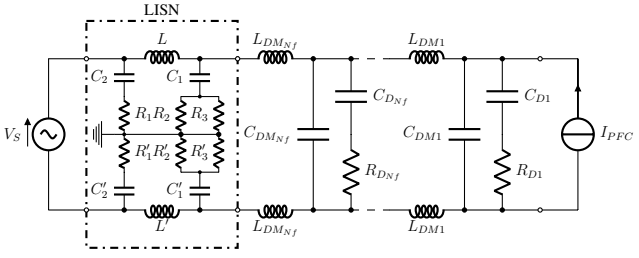


Figure 4: Simplified model for DM EMI used to determine the DM filter

$$C_{MAX} = \frac{Q_{MAX}}{Vs_{RMS} \cdot \omega s} \quad (2)$$

As described above we consider that the value of each capacitor is different for each filter stage. The largest capacitor

is placed close to the converter and the smallest capacitor is placed at the grid side (inherently treating higher frequency noise closer to the input). The filtering capacitor and the damping capacitor are considered identical within each filter stage. The distribution of the capacitor values according to the number of filter stages is defined with the following method:

$$K = \frac{1}{2} \cdot N_f \cdot (N_f + 1) \tag{3}$$

$$C_{DM_{N_f}} = C_{D_{N_f}} = \frac{C_{MAX}}{2K} \tag{4}$$

$$C_{DMi} = C_{Di} = i \cdot C_{DM_{N_f}} \Rightarrow i \in [1; N_f] \tag{5}$$

For known capacitor values, inductor values can be calculated according to the required attenuation, dimensioning frequency and product of filter capacitances, which is presented with (6).

$$L_{DM} = \frac{1}{2} \cdot \sqrt[N_f]{\frac{Att_{req}}{(2\pi f_D)^{2N_f} \cdot \prod C_{DM}}} \tag{6}$$

Middlebrook's theorem is used to determine damping resistors. The optimal damping resistor according to each filter stage elements, i.e capacitor and inductor, can be determined with the methodology presented in [16]. The damping resistor value is calculated with (7).

$$R_{Di} = \sqrt{\frac{2 \cdot L_{DM}}{C_{DMi}}} \cdot \sqrt{\frac{(2+n)(4+3n)}{2n^2(4+n)}} \tag{7}$$

"n" corresponds to the factor between filtering capacitor (C_{DM}) and damping capacitor (C_D), in this case $C_{DM} = C_D$ so $n = 1$.

As it is presented in the design flow chart (Figure 3 on page) the two system variables for C.C.M modulation are the switching frequency and the line current ripple (before filtering). The range used for the switching frequency is F_{SW} = [140 kHz ; 340 kHz] and the range for the current ripple is ΔI = [2 A ; 12 A]. Two system variables are also used for T.C.M: the switching frequency upper bound [350 kHz ; 650 kHz] and the maximal allowed reverse current (I_R) [1 A ; 3 A]. These parameter ranges were defined after preliminary optimisation. The maximal switching frequency is relatively close to the limit of SiC devices and the maximal reverse current (cf figure 11) is limited in order to control the conduction losses.

C. Semiconductors

The selection of suitable dies is made according to a database which is composed of SiC and SJ Si devices. Device volume estimation includes switch packages and driver volume (bootstrap type). The selected switch reference corresponds to the device which results in the lowest sum of conduction and switching losses in order to reduce the impact of cooling on the global volume. All semiconductor parameters used to calculate losses come from the datasheet. Regarding conduction losses, the on-state resistance at 150°C is considered, thus avoiding certain under-estimation of losses with the 25°C value. Switching losses represent a large part of the total losses: commutation times (rise time tr, fall time tf), output parasitic capacitor (Coss) and reverse recovery charge of body diodes (Qrr) are also picked from the datasheet. The turn-ON and turn-OFF energies are calculated with equations (8) and (9), respectively.

$$Esw_{ON} = \frac{1}{2} \cdot V_{DC} \cdot I_D \cdot tr + \frac{1}{2} \cdot Coss \cdot V_{DC}^2 + Qrr \cdot V_{DC} \tag{8}$$

$$Esw_{OFF} = \frac{1}{2} \cdot V_{DC} \cdot I_D \cdot tf \tag{9}$$

It is important to identify the commutation instants to estimate this type of losses, which are more difficult to obtain than conduction losses due to inherent soft commutations. During half of the grid period, one of the HF switches achieves zero voltage switching (ZVS). The second switch can also achieve ZVS if the inductor current changes its sign before the commutation. This condition occurs for high current ripple and close to the zero-crossing of the grid current as detailed in sections for C.C.M and T.C.M.

III. C.C.M Modulation

C.C.M is a fixed switching frequency modulation with variable duty cycle. Figure 5 illustrates typical current waveforms obtained with the C.C.M modulation. Most of the time, only one device turns ON in ZVS with this control. This is explained with Figure 6 on page and Figure 7 on page for the configuration corresponding to $V_s > 0$. However, soft-switching of the second switch can occur for low average current in the inductor. If Q1 is ON for long enough, the current becomes negative and so Q3 can turn-ON also with ZVS. Such switching sequences are illustrated by Figure 6 on page and Figure 8 on page . The strategy to increase the number of soft-switching instances in C.C.M is to increase the current ripple, though conduction losses are increased. Boost inductor and EMI filter losses and volumes are also widely affected by higher current ripple. The higher these two parameters (f_{SW} and ΔI), the lower the inductor value, which allows somewhat to reduce its size. However, high frequency losses, due to skin and proximity effects, will increase. The inductor value is determined according to the switching frequency and the line current ripple (cf (10)).

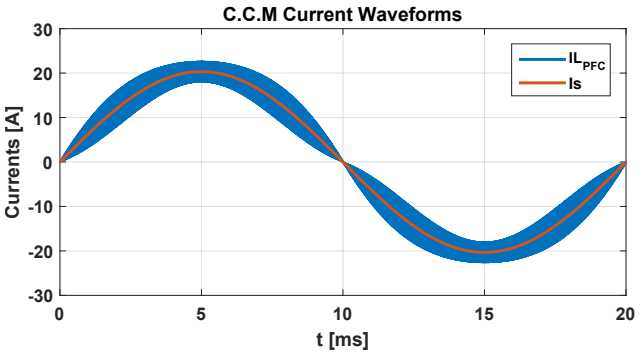
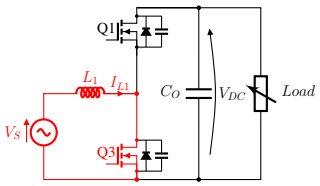
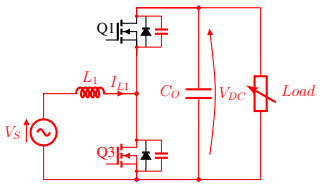


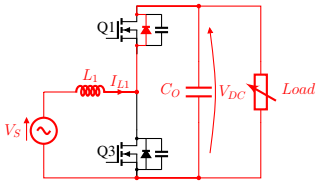
Figure 5: Inductor and line current waveforms for C.C.M modulation with f_{SW} = 140 kHz and ΔI = 6A



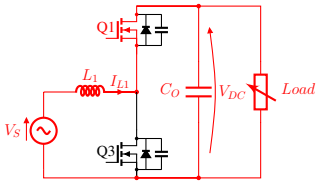
(a) Initial configuration Q3 ON and Q1 OFF, $I_{L1}$is positive and rises



(b) Q3 turns OFF, charging(Q3) and discharging(Q1) of Coss capacitors.

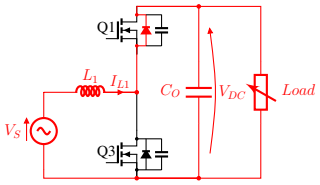


(c) Bodydiode of Q1 starts to conduct.

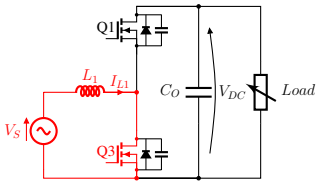


(d) Q1 turns ON in ZVS.

Figure 6: Switching sequences which are common to both cases: Q1 turns ON for I_{L1}>0.

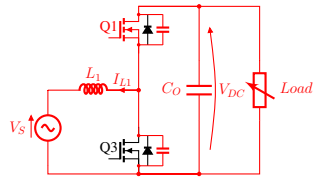


(a) Q1 turns OFF, the bodydiode starts to conduct.

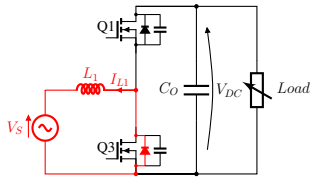


(b) Q3 turns ON, Coss capacitor is not discharged before commutation, this correspond to hard switching which involves recovery of Q1's bodydiode. Back into initial configuration.

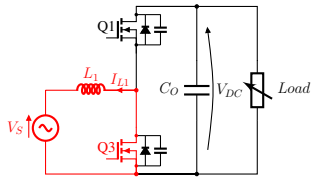
Figure 7: Switching sequence when inductor current remains positive: Q3 turns ON for I_{L1}>0.



(a) Q1 turns OFF, charging(Q1) / discharging(Q3) Coss capacitors.



(b) Bodydiode of Q3 starts to conduct



(c) Q3 turns ON in ZVS

Figure 8: Switching sequence when inductor current changes its sign during the switching period: Q3 turns ON for I_{L1}<0.

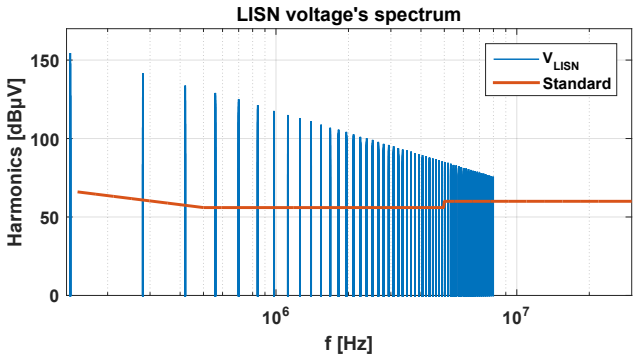


Figure 9: Fast Fourier transform of the voltage across the LISN 50Ω resistor for C.C.M modulation compared with EN55011 Standard with f_{SW} = 140 kHz and ΔI = 6A

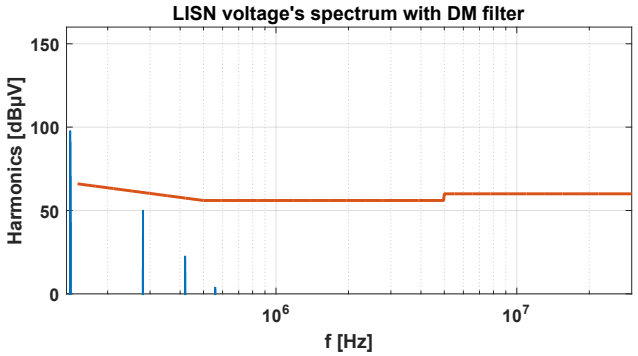


Figure 10: Fast Fourier transform of the voltage across the LISN 50 Ω resistor for C.C.M modulation compared with EN55011 Standard after the design of the DM filter with f_{SW}= 140 kHz and ΔI = 6A

$$L_{PFC} = \frac{V_{DC}}{4 \cdot \Delta Is \cdot f_{SW}} \tag{10}$$

For each couple of variables (f_{SW} and ΔIs), several inductor designs are selected to get multiple combinations with the EMI filter. For C.C.M modulation, the attenuation is obtained for multiples of the switching frequency higher than 150 kHz (lower frequency considered in the EN55011 standard). A high switching frequency allows reducing the DM filter size, as for the boost inductor. Figure 9 presents the LISN voltage spectrum before filtering. This spectrum is then used to design the EMI filter with the methodology presented in IV-B. Figure 10 allows to validate the DM filter design procedure. Thus, the designed DM filter allows to comply with the standard. The selected converter operates at 140 kHz, which is out of the EMC standard frequency band [150 kHz, 30 MHz] considered in the EMC standard. The dimensioning frequency corresponds to the second harmonic of the switching frequency.

IV. T.C.M MODULATION

T.C.M modulation is an extension of the discontinuous current mode (D.C.M); T.C.M allows inductor current to change its sign for each commutation. Figure 11 represents typical current waveforms for T.C.M modulation at nominal power. Thus, both HF switches always turn ON in ZVS.

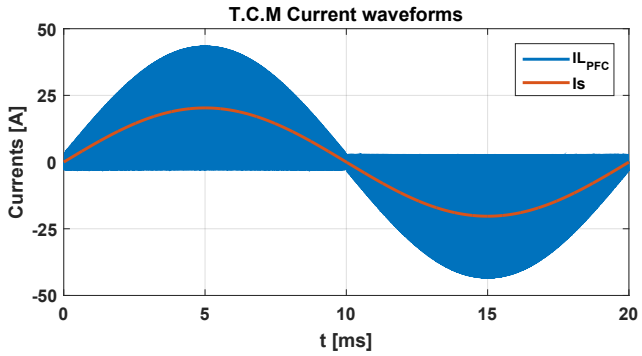


Figure 11: Inductor and line current waveforms for T.C.M modulation at 3.3 kW with I_R = -3A

The switching sequences correspond to Figure 6 on page and Figure 8 on page . The inversion of the current sign is obtained when the configuration presented in Figure 8 on page is kept for a sufficient time. A variable switching frequency is needed to obtain the required reverse current which allows the soft-switching. Some design elements are specific to T.C.M, such as dependency of inductor design on the maximal switching frequency and the minimal power. The switching frequency depends on the grid voltage and the load, increasing for lighter loads and lower voltages. The maximal switching frequency must be limited and this constraint principally impacts the boost inductor design. This modulation presents a higher RMS current than C.C.M leading to higher conduction losses in semiconductors and passives (in particular with no interleaving) e.g. input inductor and DM filter inductors.

A. Inductor value

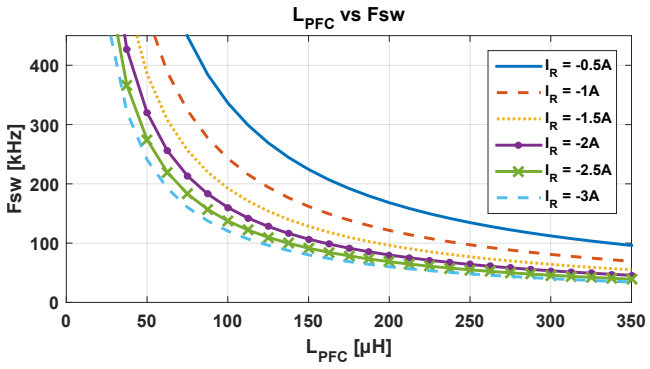
As it is mentioned above, the highest switching frequency is reached at light load. To limit the switching frequency upper bound, we considered a minimum equal to 10% of the nominal load (330 W). The corresponding inductor value can be calculated with (11). However, the inductor design must be done for operation at full load to support the higher current.

$$L_{PFC} = max\left[\frac{\hat{Vs}^2 - \hat{Vs}^2\cos(2\omega t) - \hat{Vs}\cdot V_{DC}\sin(\omega t)}{4F_{SW_{MAX}}\cdot V_{DC}(\frac{2P_{min}}{\hat{Vs}}\sin(\omega t) - I_R)}\right] \quad (11)$$

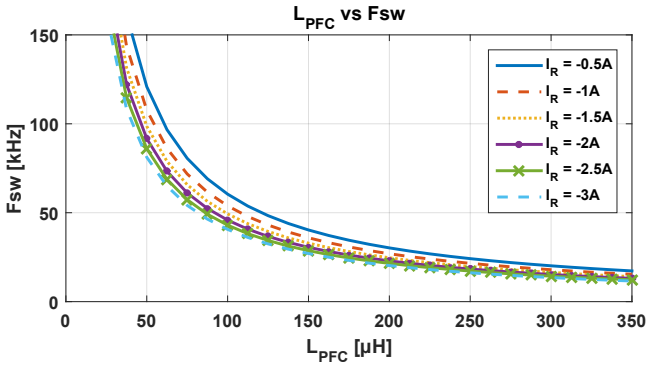
Figure 12 presents the evolution of the maximum switching frequency as a function of the input inductor, reverse current and load. For the same value of L_{PFC}, the highest switching frequency obtained at 3.3 kW is much lower than highest switching frequency at 330 W. The method presented in [17] allows to reduce the gap between the two operation point by adding a clamp circuit across the input inductor. The method can be interesting for low power converters, but is not adopted here.

B. EMI filter design

The T.C.M input current waveform contains a ripple which leads to a larger DM filter. However, for a design realized with the constraint on maximal switching frequency at low



(a)



(b)

Figure 12: Evaluation of the maximum switching frequency according to the maximum reverse current; a) 10% of the rated power; b) rated power 3.3 kW.

power, most of the spectrum at nominal power is out of the conducted emission frequency band [150 kHz, 30 MHz]. Figure 13 highlights the fact that not only standard compliance is needed with T.C.M modulation, but the variable switching frequency also widely impacts the THD due to relatively high spectrum content under 150 kHz. The DM filter cut-off frequency is therefore relatively low, which leads to a large volume. This could be alleviated by interleaving the switching frequency leg. The procedure presented in II-B is also used for T.C.M, but a second step is needed to check for THD. Once the filter is designed to be compliant with the standard, resulting in filtered noise spectrum shown in Figure 14 on page , the grid current and the THD are calculated. If the THD is higher than 5%, the filter inductor value is increased until the THD becomes lower than 5%.

V. Comparison T.C.M *vs* C.C.M

Figure 15 presents several designs for C.C.M and T.C.M modulation. Results correspond to the operation at nominal power (3.3 kW). The impact of the switching frequency can be analysed for both modulations. Regarding C.C.M, the highest density point is obtained for 140 kHz, which corresponds to the lowest switching frequency of the selected range and a current ripple of 6 A (Figure 5 on page). It can be seen that the power density is increasing continuously (180 kHz - 340 kHz). However, we can clearly see a disruption of this this trend at 140 kHz switching frequency because it falls outside

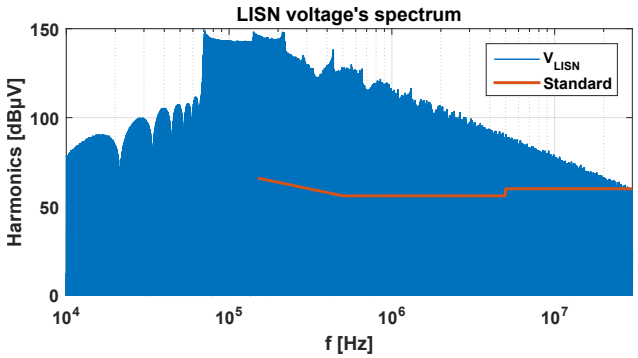


Figure 13: Fast Fourier transform of the voltage across the LISN 50 Ω resistor for T.C.M modulation compared with EN55011 Standard at 3.3 kW

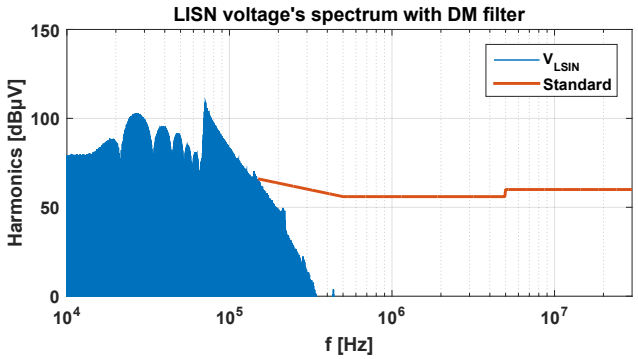


Figure 14: Fast Fourier transform of the voltage across the LISN 50 Ω resistor for T.C.M modulation compared with EN55011 Standard after the design of the DM filter. To achieve the same margin as C.C.M, the inductor value should be increased resulting in lower power density converter.

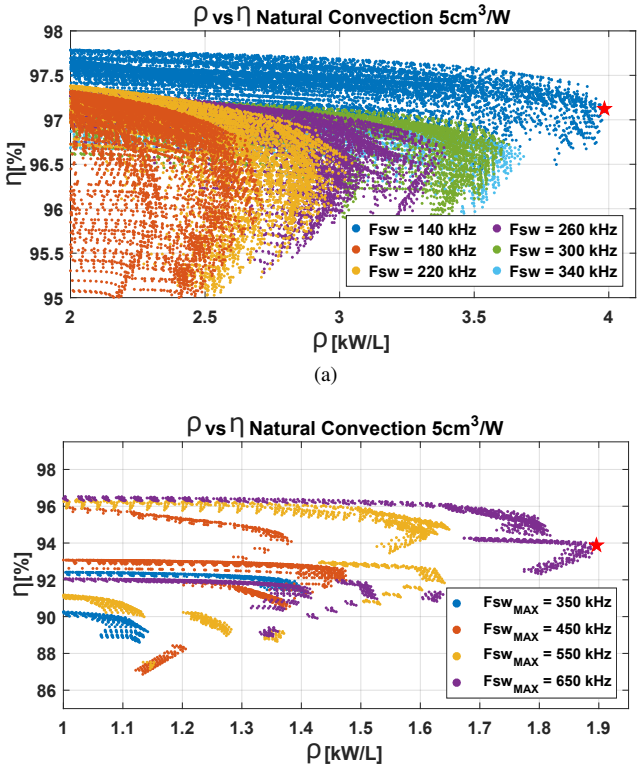


Figure 15: Representation of several converter designs in the efficiency (η) *vs.* power density (ρ) domain for various switching frequencies; a) corresponds to C.C.M modulation with design obtained for 3.3 kW; b) Corresponds to T.C.M modulation. The operation is 3.3 kW but $Fsw_{MAX}$and L_1were selected taking into account low load (330 W) capability

of the conducted emission frequency band. The design of the EMI filter is based on the second harmonic instead of the first which leads to significant filter size reduction. In the case of C.C.M, the maximum switching frequency is bound to 340 kHz because the gain on power density is not sufficient to overcome the lower efficiency. Concerning T.C.M the densest converter corresponds to a design with the highest switching frequency, 650 kHz at 330 W. This switching frequency is relatively close to the limitation of switching capabilities of SiC and SJ MOSFET.

The comparison of the two highest density converters presented in Table III on page highlights the fact that C.C.M modulation is more suitable for non-interleaved converters than T.C.M in terms of power density and efficiency. Table III allows both results to be compared in detail. In spite of the high current ripple, T.C.M switching losses are lower than C.C.M because soft switching is achieved for all operation points during the complete grid period. In both cases, SiC MOSFETs are selected. For C.C.M the selected device tends to reduce switching losses while the device selected for T.C.M presents the lowest on-state resistance of all components in the database. The thermal management (natural convection 5cm^3/W) represents an important part of the overall volume. The high current ripple of the T.C.M involves large losses in the filter which corresponds to the major part of global losses. This might be a bigger problem in a practical implementation because it is more delicate to extract heat from passive components than from active devices.

VI. Conclusion

In this paper two full bridge bidirectional PFC converters with different modulation principles, continuous current mode (C.C.M) and triangular current mode (T.C.M), were compared. Results are obtained for non-interleaved converters. They show that C.C.M is the most interesting modulation in terms of efficiency and power density, even if some commutations occur in hard condition. Operation at minimal load widely impacts the design for T.C.M. To achieve the highest density converter the switching frequency at minimal load has to be high. However, this high switching frequency combined with an important current ripple leads to a large EMI filter with important losses. Power density achieved with C.C.M is 3.98 kW/L whereas T.C.M achieves only 1.9 kW/L. It is clear that C.C.M modulation is the most suitable modulation in the case of non-interleaved converter.

To have a complete fair comparison, a new study, which includes interleaving, must be done. Interleaving techniques spread the current between several cells, which can make the

Table III: Comparison of the two highest density converters obtained for C.C.M and T.C.M modulation

		Design for C.C.M @3.3kW	Design for T.C.M @3.3kW ($F_{SW_{MAX}}$ @ P_{MIN})
General	η	97.12 %	93.87 %
	ϱ	3.98 kW/dm^3	1.9 kW/dm^3
	$F_{SW_{MAX}}$	140 kHz	650 kHz
	ΔI / I_R	6 A	-3 A
	L_{PFC}	89.28 µH	18.51 µH
	Devices	C3M0065090J(SiC)	SCT3030AL(SiC)
	Nb EMI filter stages	3	3
	L_{DM}	21.06 µH	52.31 µH
	C_{DM}	[0.33 µF,0.224 µF,0.132 µF]	[0.33 µF,0.224 µF,0.132 µF]
	L_{CM}	0.3525 mH	0.69 mH
	C_{CM}	[19.2 nF, 12.7 nF, 6.5 nF]	[19.2 nF, 12.7 nF, 6.5 nF]
Volume	Total	813.02 cm^3	321.63 cm^3
	L_{PFC}	84.24 cm^3	67.39 cm^3
	DM filter	186.18 cm^3	495.49 cm^3
	CM filter	77.58 cm^3	160.82 cm^3
	Switches+Driver	4.92 cm^3	5.78 cm^3
	Heat sink	460.1 cm^3	1010.6 cm^3
Losses	Total	95.02 W	202.12 W
	L_{PFC}	12.34 W	20.39 W
	Switches	53.45 W	45.45 W
	EMI filter	29.22 W	136.27 W

T.C.M more competitive. The EMI filter can be reduced due to lower current ripple on the line and higher apparent frequency.

The design of a prototype is presently in progress to validate the different models implemented in the design procedure.

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