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J. Le Leslé

R. Caillaud

F. Morel

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Johan LE LESLÉ*†, Rémy CAILLAUD*‡, Florent MOREL†, Nicolas DEGRENNE*, Cyril BUTTAY‡, Roberto MRAD*, Christian VOLLAIRE† and Stefan MOLLOV*

*Mitsubishi Electric R&D Centre Europe, 1 Allée de Beaulieu, 35 708 Rennes, France
†Université de Lyon, Ecole Centrale de Lyon, CNRS, UMR5005, laboratoire Ampère, 69130 Ecully, France
‡Université de Lyon, INSA de Lyon, CNRS, UMR5005, laboratoire Ampère, 69621 Villeurbanne, France

***Abstract*—This paper presents the design procedure for a Buck Power Pulsating Buffer, aimed at optimising the power density of a single phase AC/DC converter. It compares different technologies for the buffer capacitor and for the inductor with printed-circuit board (PCB) integration in mind. As ceramic capacitors are considered (X6S and Ceralink technologies), a non-linear model was developed for the capacitance and ESR variations. This differs from existing literature because film capacitors are usually used and simple models are appropriate for such technologies. Two low-cost, highly integrated inductor technologies are compared. Results allow a fair comparison of these different capacitor and inductor technologies, and it found that the design based on X6S capacitors and planar inductors offers the smaller volume and best efficiency. Moreover, the optimisation procedure favours an original approach, where the converter operates at zero voltage switching (ZVS) along the entire mains period at fixed switching frequency.**

***Keywords*—Optimisation procedure; pareto front; Power Pulsating Buffer; Electronic capacitor; ZVS; wide band-gap devices.**

I. Introduction

One of the main challenge in power electronics is to design converters with high power density [1]. The development of wide band-gap components allows reducing the volume of power converter. This is mainly due to lower losses and the high switching frequency capabilities of Silicon Carbide (SiC) and Gallium Nitride (GaN) [2]. This, in turn, allows to reduce the thermal management (because of the lower losses), and to use smaller magnetics (because of the higher switching frequency). Passive components, e.g. inductors and capacitors, represent one of the largest share of the overall converter volume, so their reduction is especially important.

In single-phase DC/AC or AC/DC applications such as Battery charger or photo-voltaic (PV), the power at the AC side can be calculated by using the voltage and the current given by (1). In these equations, it is assumed that there is no phase shift between the voltage and the current because of the Power Factor Corrector (PFC) control. From (2) it is possible to identify two components in the AC power. The first one is the DC component used by the load and the second one is the pulsating component which needs to be filtered. Usually a bulky electrolytic capacitor bank is used to filter the double line-frequency power pulsation, as illustrated in Fig. 1.

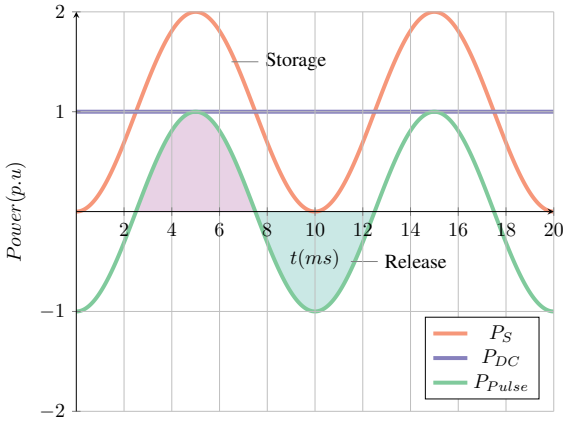


Fig. 1: Typical power waveforms for an AC/DC converter. P_S is the power on the AC side, P_{DC} is the power on the DC side and P_{Pulse} is the power that needs to be buffered by the PPB.

$$v_s(t) = \hat{Vs} \cdot \sin(\omega t) \qquad i_s(t) = \hat{Is} \cdot \sin(\omega t) \tag{1}$$

$$p_s(t) = i_s(t) \cdot v_s(t) = \frac{\hat{Vs} \cdot \hat{Is}}{2} + \frac{\hat{Vs} \cdot \hat{Is}}{2} \cos(2\omega t) \tag{2}$$

The main drawback of electrolytic capacitors is their poor reliability [3]. Moreover, the smaller the desired voltage ripple on the DC side, the larger the capacitor bank, hence a large impact on the converter volume.

To avoid electrolytic capacitors and increase the overall power density, an additional active circuit can be used (Power Pulsating Buffer – PPB – also known as electronic capacitor). The circuit is composed of a buffer capacitor used to store and release the pulsating power, Fig. 1. This decoupling method replaces the bulky electrolytic capacitors by other capacitor technologies such as film or ceramic, which offer lower capacitance density, but can sustain larger ripple currents.

The literature proposes a large number of topologies [4], [5], [6]. The different power decoupling techniques can be further

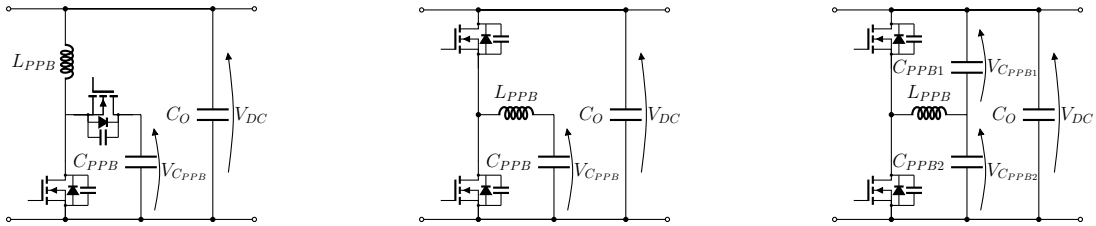


Fig. 2: Examples of different parallel Power Pulsating Buffers. a) Boost b) Buck c) Symmetrical Half Bridge (HB)

classified into several subgroups, depending on their energy storage medium, circuit configurations and control algorithms. A preliminary study identified that parallel topologies (where the PPB stage is connected in parallel on the DC bus, in a similar fashion to the electrolytic capacitor) offer the best advantages in terms of power density and efficiency for a 3.3 kW highly integrated application. Fig. 2 presents a selection of possibles parallel power decoupling circuits. In the following analysis, the inductor implemented in each topology is neglected in terms of buffering capabilities because, the stored energy in the inductor is much smaller than the energy stored in the capacitor. Fig. 2.(a) corresponds to a Boost topology [7] which means that the voltage across the buffer capacitor is higher than the DC voltage. A drawback is that this topology requires semiconductor devices with a higher voltage blocking capability that in the PFC stage. Fig. 2.(b) is a buck topology. In this case, the voltage across the buffer capacitor is lower than the DC Bus voltage. Consequently, the same switches can be used for the PFC and the PPB stages. For a buck PPB, the capacitor value can be determined according to the rated power of the PFC and the voltage excursion across the capacitor (3).

$$C_{PPB} = \frac{2 \cdot P_{DC}}{\omega \cdot (V_{PPBmax}^2 - V_{PPBmin}^2)} \tag{3}$$

According to (3) the theoretical minimal value for C_{PPB} is obtained for $V_{PPBmax} = V_{DC}$ and $V_{PPBmin} = 0$ V. An alternative to the Buck topology is the symmetrical half bridge presented in [8], Fig. 2.(c). The two capacitors implemented in this topology are used for the power decoupling and to build up the DC Bus voltage. However, the value of one single capacitor is twice as high as that of the buck for the same voltage rating, as it is shown in (4), [8].

$$C_{PPBx} = \frac{4 \cdot P_{DC}}{\omega \cdot (V_{PPBmax}^2 - V_{PPBmin}^2)} \tag{4}$$

Thus, the total capacitor requirement for the symmetrical half bridge topology is four times higher than for the buck. Among the presented power decoupling buffers, the buck proposes the lowest buffer capacitor, which is why it is preferred here. Moreover, the voltage stress on semiconductor is equivalent for the rectifier stage and the Buffer stage.

PPB circuits were used by the winner of the Google little box challenge [9]. Another finalist team [10] has shown that using the buck type PPB led to a 11.3 % overall volume reduction compared to electrolytic decoupling. Thus, the advantage

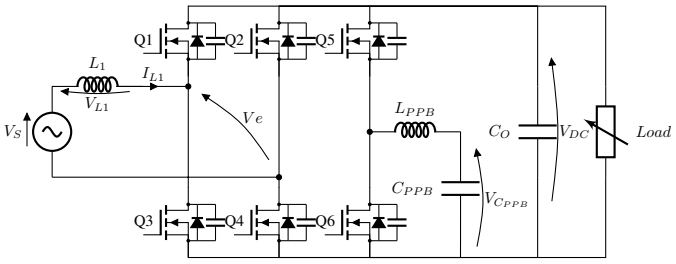


Fig. 3: A full-bridge PFC stage with the considered PPB for output decoupling

of PPB compared to a classical electrolytic DC Bus capacitor has attracted a large number of attention recently. However, one drawback of PPBs is that they require additional power switches and inductors, and generate losses. The inductor of the PPB may indeed contribute to a large share of the volume and losses. Its design is thus critical and identified as a bottleneck in the scientific community. The use of a highly integrated, low-cost, PCB-based inductor technologies has not been studied yet for this type of converter. Thus, this paper presents the optimum design of a 3.3 kW buck PPB in the context presented in Fig. 3, with a special focus on PCB integrated inductor technologies.

Section II presents the design procedure implemented for the PPB. Section III focuses on the models used in the procedure. Section IV compares results obtained for two different types of inductor. The optimised converter operates in Zero Voltage Switching (ZVS) along the complete line cycle, meaning that integrated inductors allow efficient operation with large current ripple.

II. Design Procedure

The design procedure for the PPB is similar to that presented in [11]. Fig. 4 presents it as a flow-chart. At the end of this procedure, the assessment of losses allows to determine the volume of the heat sink. This highlights the impact of the thermal management. For this project, the chosen cooling method is natural convection, considering an ambient temperature of 60°C and a maximum device temperature of 125°C (chosen as to be compatible with most passive devices, assembly and PCB technologies).

The first step in the optimisation procedure is the identification of the optimisation variables according to the application and the converter topology. For this case, the PPB is connected

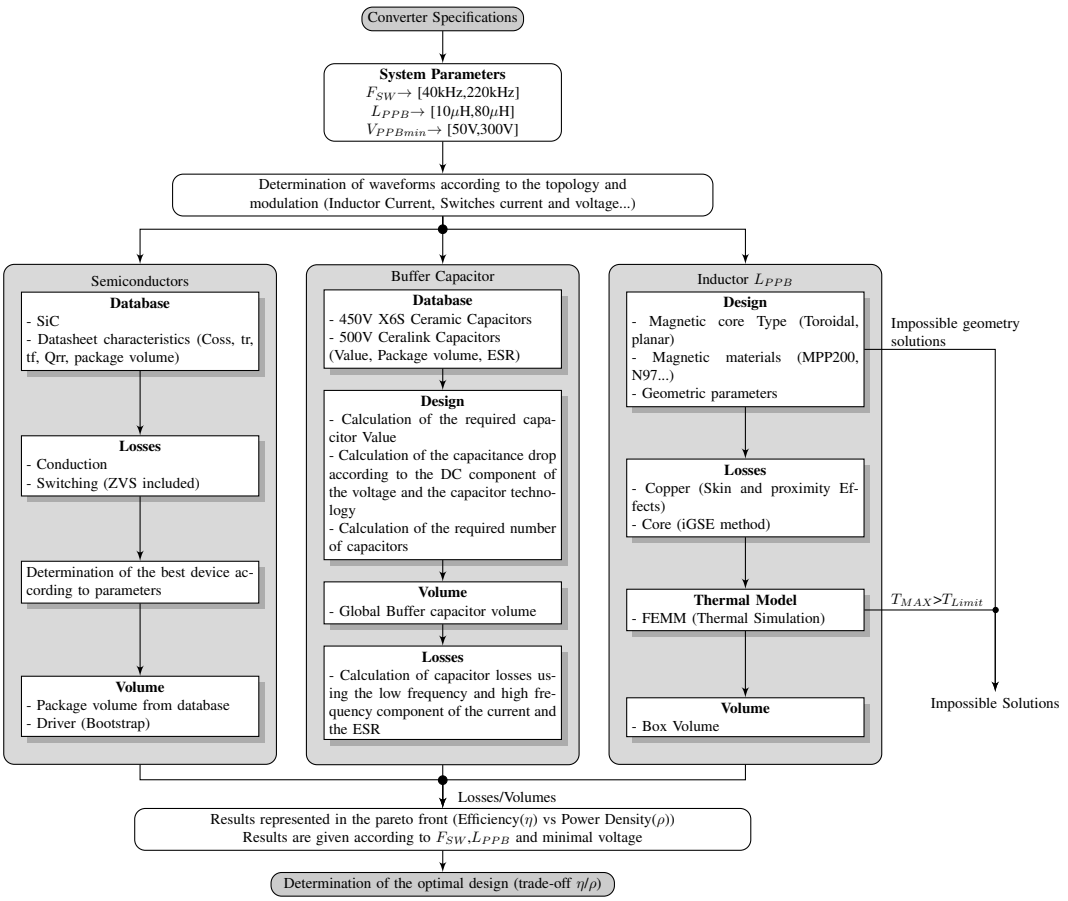
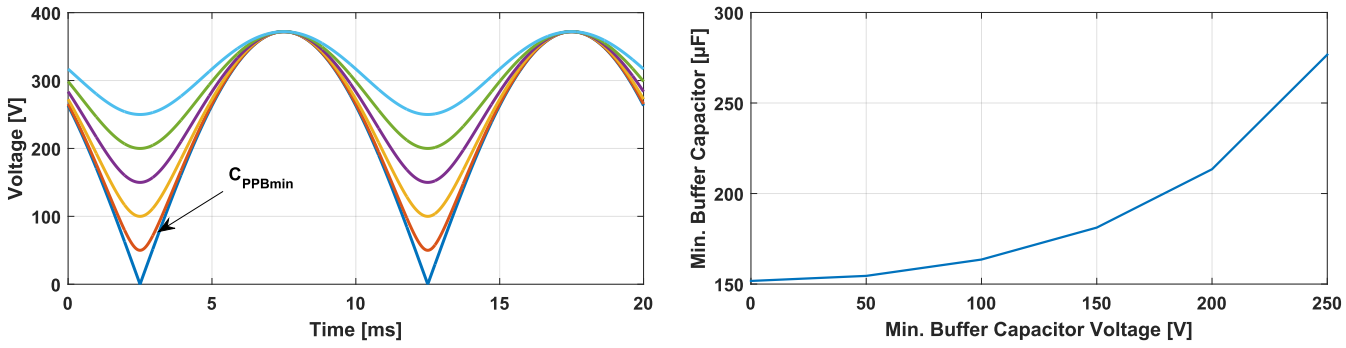


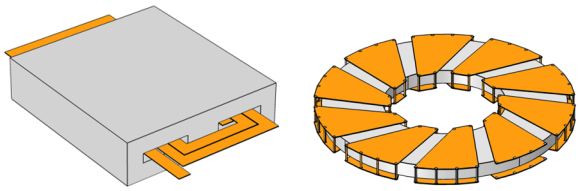
Fig. 4: Design Flow Chart presenting the optimization procedure implemented for the Buck PPB



(a) (b)

Fig. 5: Impacts of minimal voltage value a) Waveforms. b) Buffer capacitor value

in parallel to a DC bus capacitor of only 20 µF (to filter high frequency components). The DC voltage is assumed to be controlled by the rectifier stage to a value of 400V. For the optimisation procedure, three variables are used: the switching frequency (F_{SW}) of the PPB, its inductor value (L_{PPB}), and the minimum capacitor voltage (V_{MIN}). The inductor value impacts the current ripple which also impacts losses. The minimal capacitor voltage determines the required capacitor value. The maximal voltage is set at $0.93 \cdot V_{DC}$ to prevent control issues. Fig. 5 presents the relation between the minimum voltage and the buffer capacitor value. It shows that the capacitor values for minimum voltages ranging between 0 V and 100 V remain almost unchanged: C_{PPBmin} = 152 µF and $C_{PPB}(100V)$ = 163 µF. Consequently, the capacitor volume is almost equivalent for both cases. However it is preferable to keep some energy stored in the capacitor, in the case of load variations. Moreover, the higher the voltage variation across the capacitor, the higher the current flowing through it and the inductor, which negatively affects the conduction losses. The voltage across the buffer capacitor is given by (5) with "K" the security factor selected for the maximal capacitor voltage



(a) (b)

Fig. 6: PCB inductor technologies. a) Planar PCB inductor. b) PCB-embedded inductor.

(in this case $K = 0.93$). equation (5) can be derived from the expression of the energy stored in the capacitor.

$$Vc_{PPB}(t) = \sqrt{(K \cdot V_{DC})^2 - \frac{P_{DC}}{C_{PPB} \cdot \omega} \cdot (1 + \sin(2\omega t))} \quad (5)$$

III. Technologies

As it was mentioned before, high power density and integration is the main objective here. Thus, the selection of the suitable device technologies is important, as it largely impacts volume and losses. In this section, we present the chosen technologies for the semiconductors, the buffer capacitor and the inductor technologies, as well as the corresponding models.

A. Semiconductors

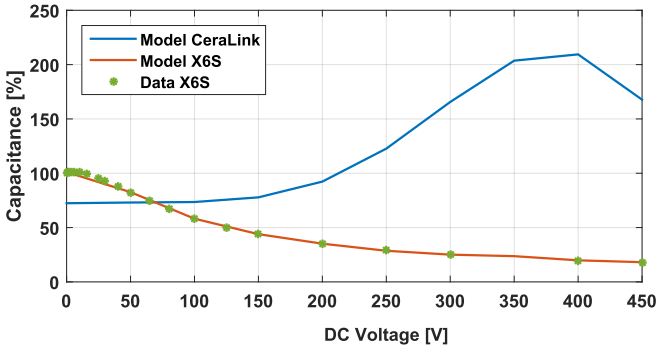
The selection of the suitable semiconductor is done among a database of SiC bare dies. The volume of a die can be neglected compared to the volume of the heat-sink required to dissipate the losses of the same die. Therefore, the semiconductor devices are selected solely on the criterion of losses minimisation. Both conduction and switching losses are taken into account. Conduction losses are calculated considering the on-state resistance at 150°C (extracted from the manufacturer's datasheet) and the RMS current value. Regarding the switching losses, datasheet parameters (tr: rise time, tf: fall time, Coss, Qrr) are also used and a simple analytical model is developed to facilitate the comparison between devices. The turn-on and turn-off energies are given by (6) and (7), respectively. As the buck topology achieves soft-switching, all commutations are analysed to identify if they lead to hard or soft switching. The necessary conditions to achieve soft-switching, in particular the impact of the inductor current ripple, are explained with more details in [11].

$$Esw_{ON} = \frac{1}{2} \cdot V_{DC} \cdot I_{SW} \cdot tr + \frac{1}{2} \cdot Coss \cdot V_{DC}^2 + Qrr \cdot V_{DC} \quad (6)$$

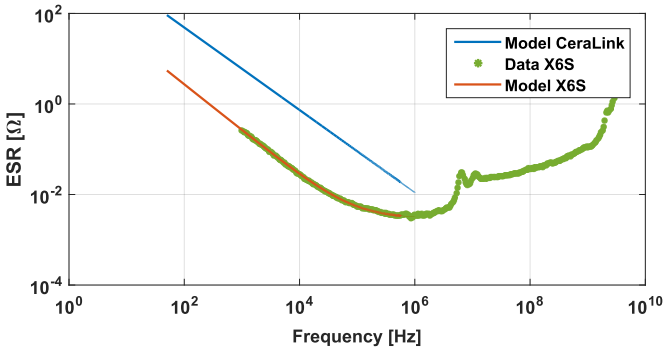
$$Esw_{OFF} = \frac{1}{2} \cdot V_{DC} \cdot I_{SW} \cdot tf \quad (7)$$

B. Inductors

Two inductor technologies are studied and compared in section IV to highlight their impact on losses and power density. In [12], Planar inductor and toroidal PCB inductor are presented and compared for a 3.3 kW interleaved PFC. All models presented in [12] are also used in this work. Both types of inductor are presented in Fig. 6. The main difference between the PFC and the PPB is the current waveform. The PFC presented in [12] uses interleaving techniques, so the average current value in its inductors is lower than for the single-stage PPB presented here. In fact, the ripple of the total current needs to be higher in the PPB to achieve ZVS. Section IV highlights the most suitable inductor type for this application.



(a)



(b)

Fig. 7: X6S and CeraLink models implemented in the design procedure, data for X6S are available thus a comparison with the model is possible a) Capacitance models. b) ESR models.

C. Capacitors

The last major part of the PPB is the buffer capacitor. Two technologies may be employed for this type of converter, film capacitors (usually used in the literature) [13] and ceramic capacitors. To allow embedding in PCB, it was decided to focus on ceramic capacitors (which can sustain larger manufacturing temperatures). Contrary to film capacitors, which are linear, ceramic capacitors can be widely impacted by parameters such as the applied DC voltage. Therefore, it is important to model the non-linear capacitor behaviour, in particular its capacitance and serial resistance (which is frequency dependent). For the considered DC bus voltage only two references of ceramic capacitors were identified (many other were discarded, mainly because of low capacitance density and/or high losses). The first one uses CeraLink technology (B58031U5105M062, TDK) and the second uses X6S (C5750X6S2W225K250KA, also from TDK).

The main characteristics for the CeraLink are available in the manufacturer's datasheet [14]. CeraLink capacitors are

made with lead-lanthanum-zirconate-titanate (PLZT) ceramic. The particularity of this technology is its capacitance increase with the DC voltage. This behaviour is really interesting and allows reducing the number of capacitors. However, its main drawback is the high series resistance at low frequency. In the case of the PPB, the large, low-frequency harmonic of the current would therefore lead to high losses. The same conclusion was also reached in [15].

The behaviour of the X6S capacitor is almost the opposite of that of the CeraLink: the capacitance decreases according to the DC voltage and the ESR is lower, in particular at low frequency. In both cases a model was developed, as presented in Fig. 7. Regarding the capacitance variation according to the DC bias, a polynomial approximation of degree 7 is used.
The ESR models are different for the two technologies. They are defined from 50 Hz to 1 MHz, which is largely sufficient for the PPB application (switching frequency lower than 500 kHz). The CeraLink can be considered linear in a logarithmic graph. The equation used is given by (8).

$$ESR_{CeraLink} = 10^{(-0.911 \cdot \log(F) + 3.511)} \tag{8}$$

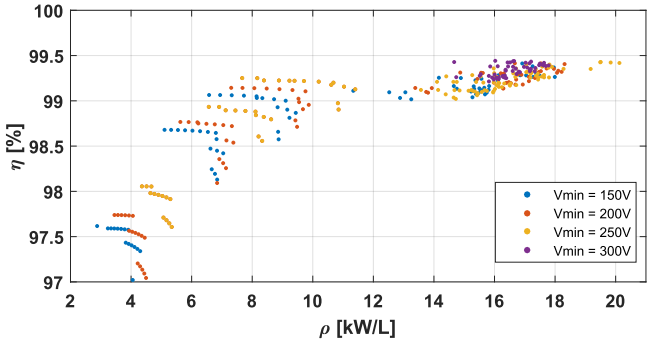
The ESR for X6S capacitor is not linear along the complete range and the linear approximation is not sufficient to estimate the ESR at the switching frequency. Consequently, the X6S ESR is modelled with a power approximation (9).

$$ESR_{X6S} = 285.9 \cdot F^{-1.011} + 0.00296 \tag{9}$$

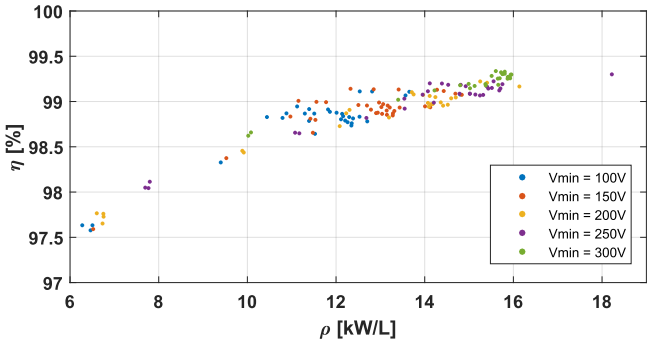
IV. Results

In the design process, many converter configurations are evaluated, and the results are presented in the power density (ρ) vs efficiency (η) domain. Fig. 8 presents some of the results for the planar and PCB-embedded inductor technologies, with a special focus on the impact of the minimum capacitor voltage. To facilitate the comparison, the results are presented in table I. Two designs are chosen on the pareto front (the set of design which offer the best ρ/η trade-off) Fig. 8.(a) and Fig. 8.(b), and these optimised PPB are simulated in more details using the PSIM software, Fig. 9. These PPBs achieve a DC Bus voltage with only ± 5 V voltage ripple. Before comparing the two PPB designs, a comparison with the classical electrolytic solution (using 47µF B43544B7476M000 from Epcos) is proposed (table I). It shows that the electrolytic capacitor generates less losses than the PPB (thus requiring no cooling system at all). However, the power density (ρ) of the PPB is much higher than the electrolytic solution.

Concerning the comparison of the two PPB designs, it is important to notice that the same configuration (F_{SW}, L_{PPB}, V_{MIN}) is obtained at the end of the optimisation, despite the use of different capacitor and inductor technologies. It is noticeable that the selected configuration tends to limit the current flowing through the inductor and the capacitor to reduce losses by increasing the minimal voltage value. In spite of the interesting behaviour of the CeraLink capacitors (capacitance increasing with the DC bias), the X6S capacitors offer a most suitable solution for this type of application. Indeed, the ESR of X6S capacitors is much lower than



(a)



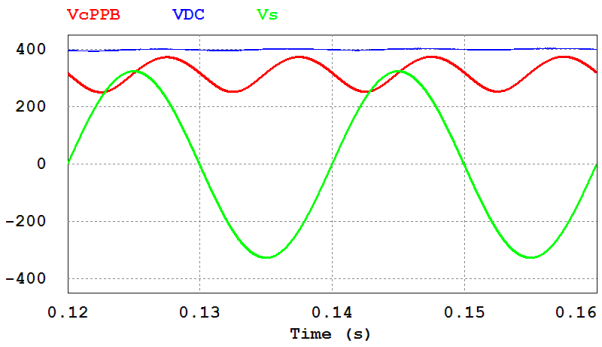
(b)

Fig. 8: Results of the optimisation presented in the Power Density vs. Efficiency domain. a) X6S capacitor/planar inductor with a thermal coefficient of 5 cm^3/W for the cooling system. b) X6S capacitor/PCB-embedded inductor with thermal coefficient of 5 cm^3/W.

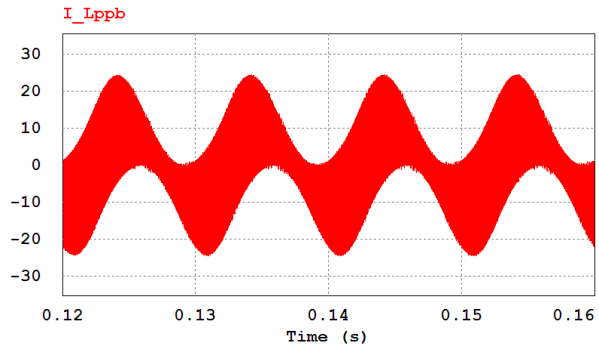
Table I: Results Comparison. Includes only box volumes

		PPB Planar	PPB PCB-emb.	Electrolytic
General	η	99.45 %	99.3 %	99.8 %
	ρ	20.12 kW/L	18.22 kW/L	3.5 kW/L
	F_{SW}	140 kHz	140 kHz	-
	L_{PPB}	20 µH	20 µH	-
	Devices	SiC	SiC	-
	C_{PPB}	277 µF	277 µF	2.6 mF
Volume	Total	167 cm^3	181 cm^3	935 cm^3
	L_{PPB}	34.04 cm^3	28.72 cm^3	-
	C_{PPB}	36.40 cm^3	36.40 cm^3	935 cm^3
	Switches	0.505 cm^3	0.505 cm^3	-
	Heat sink	96 cm^3	115.45 cm^3	-
Losses	Total	19.2 W	23.09 W	6.5 W
	L_{PPB}	10.23 W	14.12 W	-
	Switches	8.8 W	8.8 W	-
	C_{PPB}	0.17 W	0.17 W	6.5 W

with ceralink technology below 1 kHz. The current flowing through the buffer capacitor is mainly pulsating at twice the mains frequency, so low-frequency ESR is a very important parameter. Moreover, the value of the inductor is kept low to also have a large high-frequency current ripple (Fig. 9.(b)), as this current ripple permits to achieve ZVS over the full mains period. This is an original approach compared to the existing literature, in which the PPBs operate at a fixed switching frequency. Regarding the two inductor designs, the planar



(a)



(b)

Fig. 9: PSIM simulation of the optimised PPB. a) Voltage waveforms. b) Inductor current waveforms. Note that the current changes its sign during each switching period allowing ZVS.

inductor is bigger than the PCB-embedded one, but it has less losses. Consequently, the global volume is higher for the PCB-embedded solution because it requires a bigger heat sink. In fact, it can be said that the planar technology seems to be more suitable for this application, but this must be verified experimentally, as many assumptions were made to simplify the design process.

V. Conclusion

In this paper, we presented the optimisation procedure for a parallel buck power pulsating buffer, based on simple models for semiconductors and passives. Two types of ceramic capacitor are identified, using CeraLink and X6S technologies. It is found that the X6S capacitors offer better performances than CeraLink, because of their lower ESR at low frequency (below 1 kHz). Two PCB inductor technologies, planar and PCB-embedded, are also presented and compared. The conclusion of this comparison is that the planar solution leads to best performances (smaller volume, less losses) than the PCB-embedded solution. This is due to the size of the thermal management system: a larger heatsink is required to dissipate the additional losses for the PCB-embedded inductor, resulting in a larger global volume. In any case, it is noticeable that PPB converters allow a dramatic gain in power density compared to a classical electrolytic capacitor solution. This remains true even when using natural convection, where the larger losses directly result in larger heatsink and tend to increase the converter volume. Power Pulsating Buffers are one of the best solutions when the power density is the main objective. The perspective of this work is the experimental test of the designs presented here, to validate the models and check if the planar structure is indeed the best solution here.

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