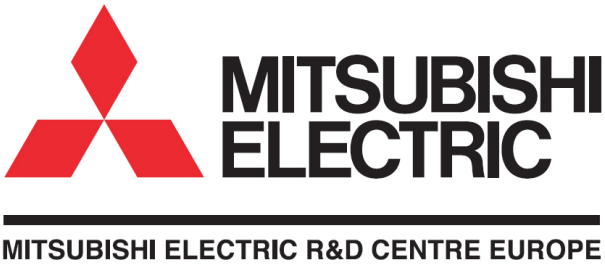


2018 IEEE Energy Conversion Congress and Exposition (ECCE)

DOI: 10.1109/ECCE.2018.8557880

A Gate Driver Based Approach to Improving the Current Density in a Power Module by Equalizing the Individual Die Temperatures

Jeffrey Ewanchuk

Julio Brandelero

Stefan Mollov

A Gate Driver based Approach to Improving the Current Density in a Power Module by Equalizing the Individual Die Temperatures

Jeffrey Ewanchuk, Julio Brandelero, and Stefan Mollov
Power Electronic Systems Division
Mitsubishi Electric Research Centre Europe
Rennes, France
j.ewanchuk@fr.merce.mee.com

***Abstract*— the current sharing in a high current power module can be uneven, and thus, the current handling capability of that power module does not correspond to the sum of the dies capability. Hence, in the effort to improve the utilization of the individual dies within a power module, this paper explores a gate driver based approach which aims to equalize the internal junction temperatures of its composite dies. The implementation of the die-level junction temperature estimation, the generation of a target temperature reference and the selective die activation to control the individual die losses is presented as the key enabling elements for the proposed gate driver and power module. Experimental results confirm the reduction in the peak die temperatures, and consequently, the current output is shown to be able to increase by a factor of 20%.**

Keywords—Multi-die power module, gate driver, SiC devices, reliability, thermal control

Fig. 1. INTRODUCTION

High current power modules are a fundamental enabling technology for applications such as offshore wind converters, and high voltage DC transmission systems. Consequently, as these applications are seeing an increased deployment due to the continued focus on renewable energy, high current power modules are naturally under developmental pressure to increase their power density and reliability [1].

Parallel-connected devices, i.e. IGBT modules or dies, suffer from current unbalances, which inevitably lead to thermal unbalance issues [2-4]. One contributing factor is due to the variation in the threshold voltages across the parallel dies, although screening can limit the impact of this issue [2]. Another contributing factor is the layout of the dies within the power module, and the parasitic inductive loops between the dies, requiring large gate resistances and careful design for proper mitigation [3, 4].

Owing to these issues, multiple techniques have been proposed to limit the unbalance of current between power modules. A balancing controller for parallel connected IGBTs has been implemented via delayed gate pulses [5, 6]. Using variable gate delay pulses to control the parallel devices has also been illustrated for SiC MOSFETs, particularly with a differential current transformer to detect the unbalanced drain current [7].

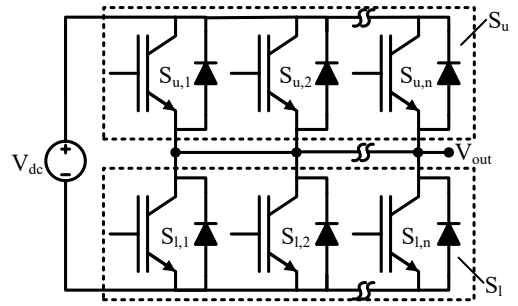
Active thermal control of parallel connected converters has also been explored to mitigate non-ideal current sharing [8]. Furthermore, active thermal control techniques can be implemented in a number of ways, i.e. using controlled shoot through [9], pulse-width modulation patterns [10], reactive power circulation [11], or via gate voltage modulation [12-14]. Typically, these active thermal control techniques improve the lifetime of the converter by lowering the magnitude of the junction temperature swing, i.e. by increasing the minimum junction temperature [15].

This paper describes the use of a gate driver-based technique, which employs individual die temperature balancing to achieve an increase in the power density of a power module. While this technique is enabled through the use of a multi-die power module with individual gate access, the power module is internally regulated by a selective gate driving (SGD) approach. This regulation is the outcome of three components and hence, each section of this paper deals with each item accordingly. The first section details the internal junction temperature measurement system for a multi-die power module. Secondly, as the proposed technique is required to be independent of the power load level, a method for generating the internal reference temperature for the inter-die temperature regulation is detailed. Third, the approach to equalize the die temperatures by a means of selectively driving the multi-die power module is described. Finally, the implementation on an FPGA is described for an integrated solution. Experimental results confirm the operation of the proposed gate driver and steady-state measurements illustrate a balanced temperature profile on the multi-die power module, effectively enabling a higher output current with the same temperature variation.

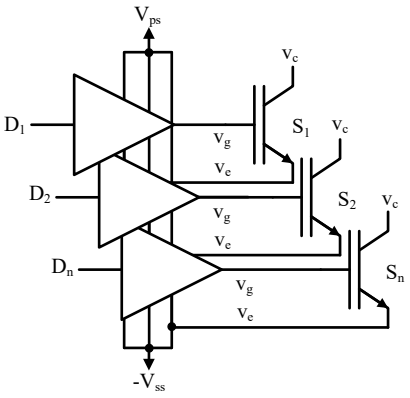
Fig. 2. PRINCIPLE OF OPERATION

A multi-die power module is depicted in Fig. 1 (a), where 'n' parallel IGBT dies form the upper and lower switches, S_u and S_l respectively. While a multi-die power module typically

has each die connected to a single gate pad, an alternative



(a)



(b)

approach has the gate pads with individual contact points, thereby minimizing the gate loop inductance and the overall switching losses [3, 16]. A further benefit to having individual gate connections in a power module is the ability to drive each parallel device independently. This concept called 'selective gate driving' has been demonstrated for SiC MOSFET power modules, and has illustrated an extension of the power module lifetime, albeit by using a pre-calculated switching pattern to compensate for any thermal unbalances rather than feedback from the junction temperatures of the internal dies [17].

In this paper, selective gate driving is employed in conjunction with a per-die thermal regulation technique to eliminate the hotspots and improve the current density of a high current power module. Compared to previous work, the key difference in this paper is that a temperature estimation routine is used as feedback in the controller, as opposed to estimating the required power profile based on a pre-calculated thermal model.

The thermal regulation system is shown in Fig. 2, where the externally applied PWM duty cycle is modified by a controller to produce a specific power profile to each die based on the feedback of the internal junction temperatures in the power module. With a given PWM input, the switching and conduction losses are incurred in a die i.e. $P_{sw} + P_{cond} = P_{tot}$. These losses, i.e. [P], are injected into the power module plant model, as shown in Fig. 2, giving the output temperature profile [T]. By controlling the specific timing of each die relative to one another, the specific losses of the dies, [P], can

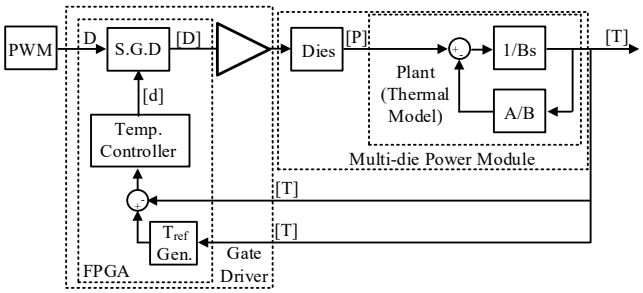


Fig. 2. Control schematic of the Selective Gate Driven

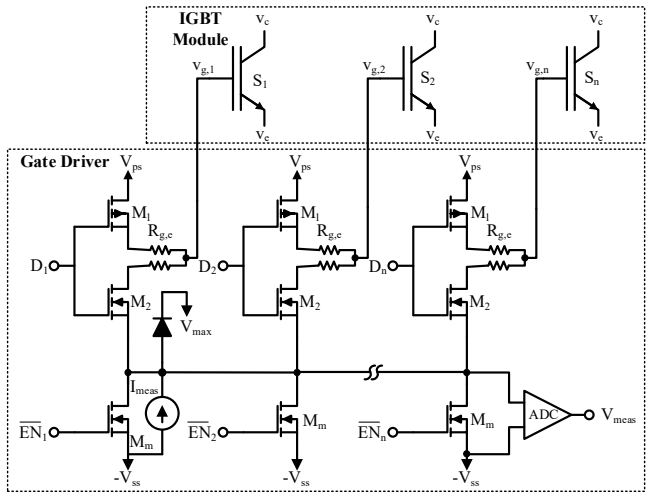
be modified to produce an objective temperature profile [T], such that $T_1 \approx T_2 \approx \cdots \approx T_n \; \forall \; t$ based on the measured die temperatures. Therefore, this paper is presented in four components: One, the technique for estimating the junction temperature used as feedback for the controller. Two, the generation of the internal reference temperature from the measured junction temperatures. Three, the modulation of the losses in the power module according to a temperature difference. Four, the controller implantation in the selectively driven power module. Note that the control loop dynamics and stability of the thermal system are intended to be the subject of another work, but are found to be not problematic due to the large thermal time constant of the system employed.

a. Estimation of the Junction Temperature

Fundamentally, a balanced temperature profile requires information of each individual junction temperature. While a multitude of junction temperature methods exist, using temperature sensitive electrical parameters, TSEPs, have been shown to be best suited to on-line operation due to their inherent non-local? temperature indication. Furthermore, among the possible TSEPs, the internal gate resistance is an appealing parameter due to the lack of interaction with the power terminals on the power module [18, 19].

In the proposed technique, a pulse injection circuit, as shown in Fig. 3 (a), is employed to estimate the internal gate resistance, as shown in Fig. 3 (b), by sampling the gate voltage immediately after the pulse injection circuit is applied, as shown in Fig. 3 (c). Owing to the selective gate drive technique, a single die in the parallel set of dies can be deactivated for a single switching cycle. Using the die in the off-state with the other dies in on-state, has the added value of allowing the ADC to be referenced from the negative gate voltage rail, simplifying the power supply design for the conversion chain. Furthermore, the input capacitance of the IGBT remains constant in the negative voltage region [18]. Hence, for the purposes of this paper, the die measured is done in the off-state of the device, though similar approach can be adopted for the on-state of the dies..

After an external request from the controller for a temperature measurement on a specific die, a pulse current is injected, and the gate voltage increases linearly, as shown in Fig. 3 (c), according to (1). At the initial injection time, the gate voltage is equal to the measurement current, and the



(a)

(b)

(c)

Fig. 3. Individual gate buffers with DC current injection to

temperature sensitive gate resistance, via (2). In this case, the capacitor voltage on C_{ies} is approximately zero due a small sampling delay or large input gate capacitance. However, in the case where the sampling delay is not negligible, or due to ringing effects on the gate voltage, two samples can be taken at times t_1 and t_2 in order to approximate the gate voltage at the initial injection time, as per (3). Nonetheless, the sampled gate voltage then provides an estimation of the junction temperature by establishing the linear parameters A and B through a calibration step.

$$V_{ge}(t) = R_g(T)I_{meas} + t \cdot \frac{I_{meas}}{C_{ies}} \quad (1)$$

$$V_{ge}(t_1) \approx R_g(T)I_{meas} \quad (2)$$

$$V_{ge}(t_1) \cdot \frac{t_2}{t_2 - t_1} - V_{ge}(t_2) \cdot \frac{t_1}{t_2 - t_1} = R_g(T)I_{meas} \quad (3)$$

$$T_{j,est} = A \cdot V_{meas}(T) + B \quad (4)$$

While the sensitivity of the junction temperature method to the variation in sampling time, I_{meas} and V_{meas} limits the accuracy of the method, it has been shown in previous work that estimations of approximately 1°C are possible [20]. After the measurement of the temperature in a specific die, the controller can freely move to the next die in the power module. In this fashion, the selected die is de-activated, and the remaining dies assume the load current for the sampling period of the temperature. As the neighboring dies remain in a conducting state, the range of the voltage is limited and the change in input capacitance is negligible.

b. Generation of the Reference Temperature

The second aspect in developing a balanced thermal profile for the multi-die power module involves generating a reference temperature for the controller, such that it is independent of the loading condition. Considering the internal gate resistance as the TSEP, two approaches are possible: one method, injects measurement current into all dies simultaneously during an off-state, as shown in Fig. 4 (b). In the latter method, the average temperature across all the dies is inherently measured owing to each gate resistance being in parallel during the measurement. In a second method, as shown in Fig. 4 (a), the average temperature is determined based on the sample of each sequential die, i.e. $T_{ref} = \Sigma T_n(k-n)/n$, where 'k' is the sample number and 'n' is the number of dies.

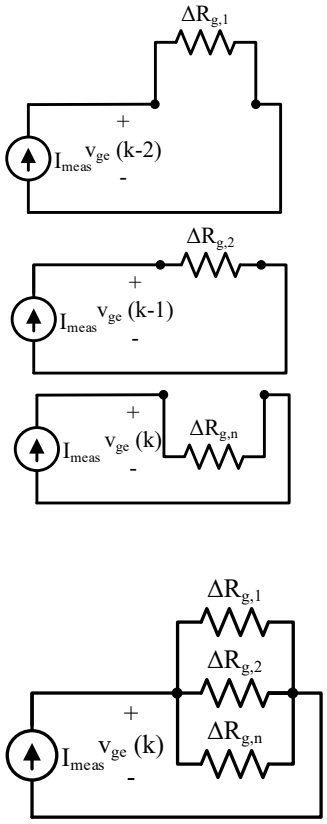
Considering the first method, where the average temperature is estimated at one sampling instance by measuring all the gate resistances in parallel, the main drawback is the reduced sensitivity of the TSEP. As the temperature estimation method relies on the change in gate resistance as a function of the temperature, $\Delta R_g \cdot T$, more gate resistors in parallel imply that the sensitivity is reduced to $\Delta R_g \cdot T/n$. Furthermore, as the input capacitance, C_{ies}, is dependent on the blocking voltage, a more complex calibration procedure would be required.

In this paper, the method where the average junction temperature is calculated in real-time by a history of the die temperature samples. A drawback of this method is that the control bandwidth is limited to the sampling rate of the die temperatures, and the number of dies, as per (5). However, as the sampling rate, f_s, is equal to the switching frequency, f_{pwm}, the control bandwidth is sufficient to track changes in the temperature, as the smallest thermal time constant in the experimental power module is on the order of 100us. Hence, the reference temperature for the parallel set of dies can be determined independent of the loading condition.

$$BW = \frac{f_s}{2 \cdot n} \quad (5)$$

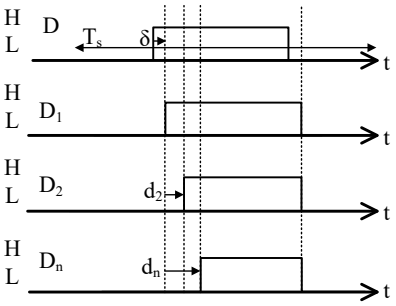
c. Power Loss Modulation

Based on the difference between the generated reference temperature, and the specific junction temperature of a die, an error is generated that is processed by a controller, as shown in Fig. 2. The controller calculates the required edge delay/advance of each die, such that the selective gate drive

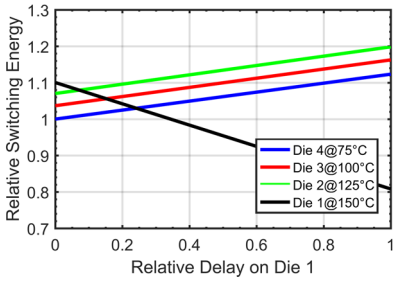


(b)

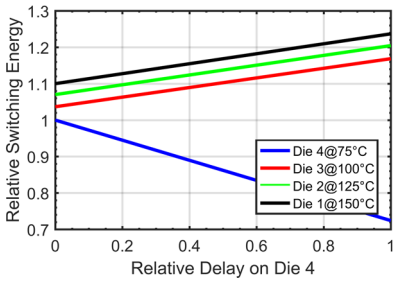
Fig. 4. Generation of the reference temperature: (a) constructing the average temperature based on the



(a)



(b)



can modulate the power losses and balance the temperatures within the power module. This section describes the translation of the temperature error to the die driving profile, such that a power loss profile is achieved.

The FPGA within the selectively driven power module captures the rising/falling edges of the input PWM signal, and within a delay time of δT_s, processes the required activation delay for each respective die based on the measured temperature error. By delaying the turn-on or advancing the turn-off time, the controller determines which dies commutate the current during the switching dynamic, thereby modulating the power losses. Considering the turn-on switching edge, the relative gate pulses for 'n' dies is shown in Fig. 5 (a), with die 'D_2' delayed by d_2 relative to D_1. In this example, D_2 commutates after D_1, and experiences less switching losses as the overlap between the falling V_{ce} and I_C is smaller. Note that advancing the switching edge manipulates the turn-off switching losses, and increasing delay can also be used to manipulate the conduction losses.

The strategy employed therefore uses the coldest die in the power module as the reference, and the relative delay to the input PWM is the non-ideal delay δT_s, i.e. $d_{cold} = 0$. The dies with a higher measured temperature are then delayed relative to the coldest die, thereby causing the temperatures to decrease in the hotter dies, and increase in the coldest die. So long as the delay is still within the discharge time of V_{ce}, the total losses remain relatively fixed, with the decrease in switching losses of the hottest die being re-distributed to the increase in losses of the coldest die. As an example, the turn on switching energy for four parallel MOS gate power devices is shown in Fig. 5 (b) and (c), with the respective junction temperatures of $150°C, 125°C, 100°C$ *and* $75°C$. Normally, with no delay, the hottest die conducts first, causing it to have the largest switching energy. Increasing the delay of the hottest device, as shown in Fig. 5 (b), linearly decreases the switching energy, and linearly causes the colder dies to increase their respective switching losses. At roughly 20% relative delay, the formerly hottest die has the same switching losses as the coldest die in the set. However, delaying the coldest die, as shown in Fig. 5 (c), only results in a decrease in switching energy of the die with the lowest switching losses. Hence, so long as the hottest die is targeted, the hottest die power losses can be controlled, as per (6), along with the coldest dies, as per (7), where the losses and delay are related by a linear factor K_T.

$$\Delta P_{loss,hot} = -K_T \cdot d_{hot} \quad (6)$$

$$\Delta P_{loss,cold} = \frac{K_T}{n} \cdot d_{hot} \quad (7)$$

The implementation of the control strategy therefore concentrates on the control of the hottest die relative to the colder dies in terms of applied delay in the gate voltage logic. A summary of the control process loop for equalizing the die temperatures is shown in Fig. 6. Using the method described in Section II. B, the reference temperature is initially calculated, and then compared against the last reference temperature sample to determine if it is larger than the allowed temperature deviation α_1. The temperature deviation limit α_1 is required to ensure that the reference dynamics are within the allowable bandwidth for controllability. Secondly, sampled junction temperatures of each die are then sorted, and the maximum and minimum die temperatures are identified, along with the corresponding die. The coldest die is used as the delay reference, and if the temperature deviation between the hottest and coldest die is larger than α_2, the hottest die is delayed. The temperature deviation limit α_2 is required to avoid trying to regulate the die temperatures below the precision of the temperature estimation accuracy limit, i.e. 1°C. Finally, the delay on the hottest die is calculated according to a controller, G_C, i.e. a proportional controller with $G_c = K_p$, so long as this delay is less than d_{max}. The process loop then continues with a new die being the hottest die, and continuing until all the dies converge into the reference temperature.

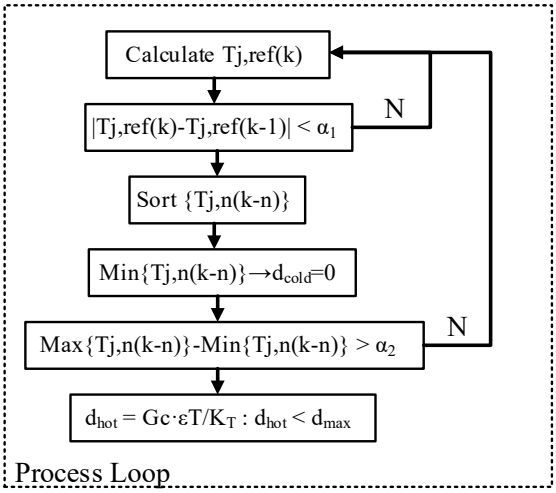


Fig. 6. Temperature regulation process loop for equalizing the die temperatures by the application of a delay/advance in the individual die gate voltage logic

d. FPGA Implementation

The process loop is implemented with an FPGA unit that is able to calculate the drive logic for each die. This calculated delay is based on the detected rising/falling edge of the input PWM. Furthermore, this edge detection is used as a process trigger for several tasks within the FPGA, i.e. sampling frequency for the temperature. In addition, the FPGA communicates with the analog to digital converter, and requests a specific die to be sampled, as shown in Fig. 7.

The sample request is handled by enabling a specific MOSFET in the gate driver through the EN_n signal, as shown in Fig. 3 (a). Once a sample is made via V_{meas}, it is converted to an actual temperature via the calibration step. Each die temperature is saved within a register for use in calculating the reference temperature, and also to determine the maximum and minimum temperatures in the parallel set of dies. A master temperature controller is therefore responsible for issuing the temperature requests, and calculating the specific delays required to equalize the die temperatures. With a specific delay calculated, i.e. as per the process loop in Fig. 6, the timer unit at the FPGA clock frequency generates the specific delay for each die. Finally, the specific driving logic [D] is applied to all gates simultaneously, via the selective gate driving stage. The overall top layer schematic of the FPGA implementation is depicted in Fig. 8.

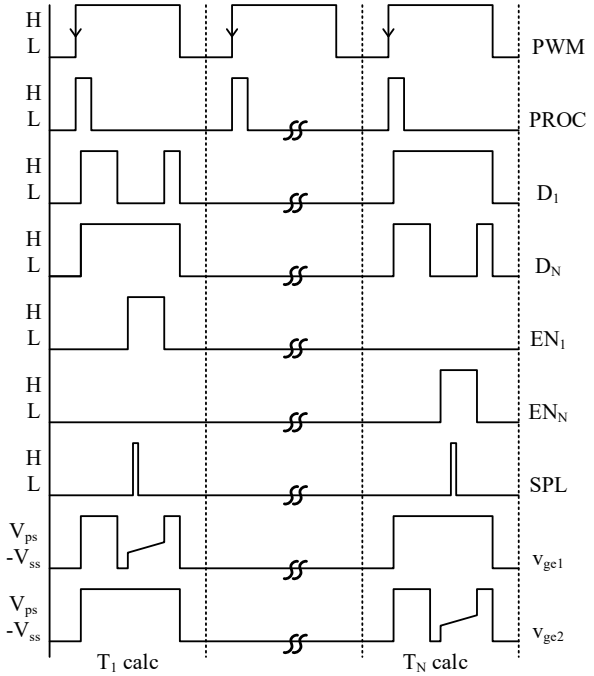


Fig. 7. FPGA process timing for measuring individual

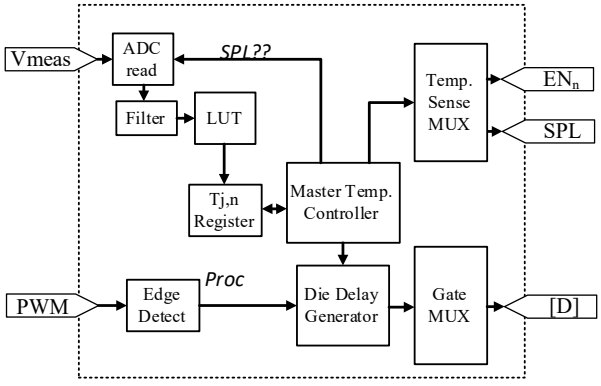


Fig. 8. FPGA top layer implementation with logical units

Fig. 3. EXPERIMENTAL RESULTS

In order to validate the proposed selective gate driving technique, a mock prototype was developed using 2 parallel

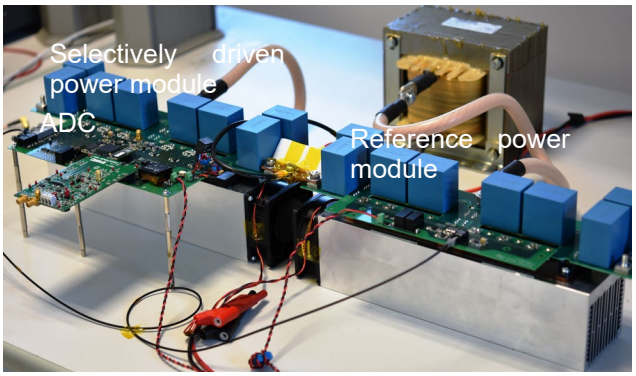


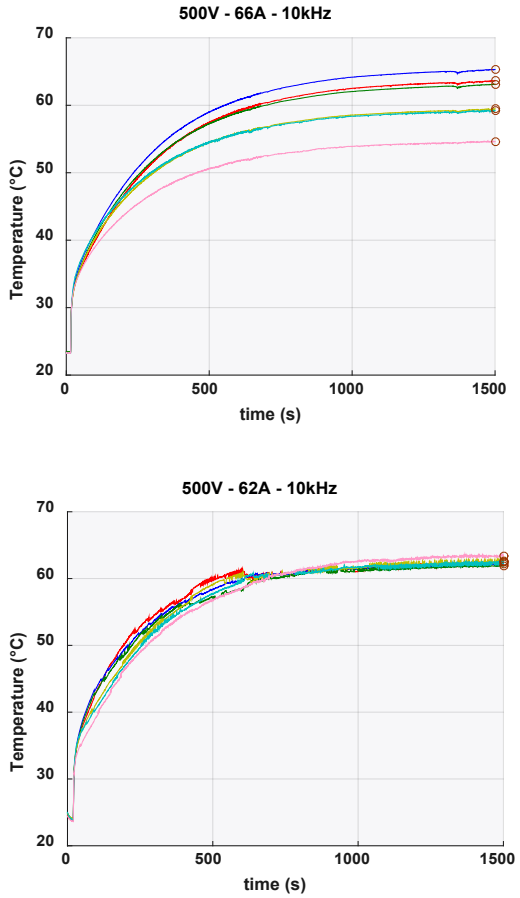
Fig. 9. Experimental prototype of the proposed gate driver

six-pack IGBT modules, CM150TX-24S1, in order to create 6 parallel devices in total, as shown in Fig. 9. While the FPGA and corresponding individual gate buffers are intended to be part of an integrated solution for intelligent power modules, the prototype is intended to only demonstrate the functionality of the concept with discrete components. The FPGA employed for prototype is a Xilinx Spartan-6 with a 100 MHz clock, paired with a 16-bit AD7626 ADC.

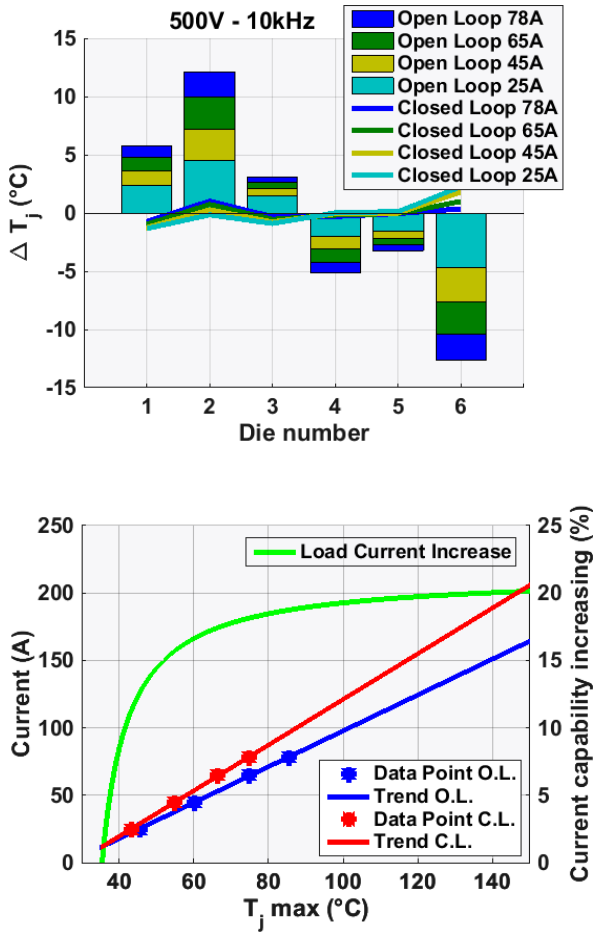
In order to load the prototype module, another power module was developed based on the same parallel connection of the CM150TX-24S1 power module. In order to provide a reference case, this power module was constructed with a single gate buffer to drive the six-dies. With a Labview Real-time controller providing the reference PWM signal, a DC current was controlled through a load inductor between the selectively driven power module and the single gate driven power module. A DC voltage of 500V, a switching frequency of 10 kHz, with the capability of circulating up 100A. Each synthetic power module is actively air-cooled, leading to a large thermal unbalance across the set of parallel dies due to cooling asymmetries.

Under the presented experimental conditions, the base-line temperature distribution across the 6 dies is shown in Fig. 10 (a), under open-loop (no control) with the difference from the hottest and coldest die being approximately $9°C$. By enabling the thermal regulation of the selectively driven power module, the resultant temperature distribution is shown in Fig. 10 (b), with the difference from the hottest and coldest die being reduced to less than $0.5\,°C$. Note that Fig. 10 represents operation of the selectively driven power module from zero to full load, and the maximum difference between the temperatures of the dies remains below 4K under these dynamic conditions.

Furthermore, comparing the operation at steady-state under variable loading conditions, the selectively driven power module is able to reduce the peak junction temperature from a maximum difference of 25K to under 2K, as shown in Fig. 11 (a). Note that the coldest die, die '6' has increased temperature, whereas the hottest die has reduced its temperature to match the mean temperature. The differences between these operating conditions can be further visualized for a given maximum temperature, as shown in Fig. 11 (b). Hence, for a given current, there is a reduction in the peak junction temperature. Similarly, it can also be seen that for a fixed junction temperature, the current capability of the power module increases as there is now extra margin in the junction temperature of the hottest die. Therefore, assuming a power module limited by the maximum junction temperature of the hottest die, the experimental results confirm an increase of 20% in the total current handling capability of the power module due to the proposed gate driver approach.



(b)



(b)

Fig.11. Comparison of the selectively driven power module with (a) absolute temperature difference comparing the open loop results, and two methods of temperature

Fig. 4. CONCLUSION

In this paper, a gate driver based approach for a multi-die power module with internal temperature regulation was presented. The methodology for measuring the per-die junction temperature, calculating the reference temperature, operation of the controller and the implementation on a FPGA was detailed. Through an experimental prototype, it was shown that by balancing the internal junction temperatures, the current capability of the power module could be increased by 20% for the same number of dies. Furthermore, for a fixed current, the peak junction temperature can be significantly reduced, and thereby increasing the reliability of the power module.

Fig. 5. REFERENCES

[1] P. Ning, F. Wang and D. Zhang, "A High Density 250C Junction Temperature SiC Power Module Development," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 2, no. 3, pp. 415-424, Sept. 2014.

[2] X. Wang, Z. Zhao and L. Yuan, "Current sharing of IGBT modules in parallel with thermal imbalance," 2010 IEEE Energy Conversion Congress and Exposition (ECCE), Atlanta, GA.

[3] M. Wang, F. Luo and L. Xu, "An improved wire-bonded power module with double-end sourced structure," 2016 IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, 2016.

[4] Y. Tang and H. Ma, "Dynamic Electrothermal Model of Paralleled IGBT Modules With Unbalanced Stray Parameters," in IEEE Transactions on Power Electronics, vol. 32, no. 2, pp. 1385-1399, Feb. 2017.

[5] P. Hofer, N. Karrer and C. Gerster, "Paralleling intelligent IGBT power modules with active gate-controlled current balancing," PESC Record. 27th Annual IEEE Power Electronics Specialists Conference, Baveno, 1996.

[6] R. Alvarez and S. Bernet, "Sinusoidal Current Operation of Delay-Time Compensation for Parallel-Connected IGBTs," in IEEE Transactions on Industry Applications, vol. 50, no. 5, pp. 3485-3493, Sept.-Oct. 2014.

[7] Y. Xue, J. Lu, Z. Wang, L. M. Tolbert, B. J. Blalock and F. Wang, "Active current balancing for parallel-connected silicon carbide MOSFETs," 2013 IEEE Energy Conversion Congress and Exposition, Denver, CO, 2013.

[8] C. J. J. Joseph, M. R. Zolghadri, A. Homaifar, F. Lee and R. D. Lorenz, "Novel thermal based current sharing control of parallel converters," INTELEC 2004. 26th Annual International Telecommunications Energy Conference, 2004, pp. 647-653.

[9] A. Soldati, F. Iannuzzo, C. Concari, D. Barater and F. Blaabjerg, "Active thermal control by controlled shoot-through of power devices," IECON 2017 - 43rd Annual Conference of the IEEE Industrial Electronics Society, Beijing, 2017, pp. 4363-4368.

[10] D. Kaczorowski, M. Mittelstedt and A. Mertens, "Investigation of discontinuous PWM as additional optimization parameter in an active thermal control," 2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe), Karlsruhe, 2016.

[11] D. Zhou, F. Blaabjerg, M. Lau and M. Tonnes, "Thermal Behavior Optimization in Multi-MW Wind Power Converter by Reactive Power Circulation," in IEEE Transactions on Industry Applications, vol. 50, no. 1, pp. 433-440, Jan.-Feb. 2014.

[12] P. K. Prasobhu, G. Buticchi, S. Brueske and M. Liserre, "Gate driver for the active thermal control of a DC/DC GaN-based converter," 2016 IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, 2016, pp. 1-8.

[13] B. Wang, L. Zhou, Y. Zhang, K. Wang, X. Du and P. Sun, "Active Junction Temperature Control of IGBT Based on Adjusting the Turn-off Trajectory," in IEEE Transactions on Power Electronics, vol. 33, no. 7, pp. 5811-5823, July 2018.

[14] Liang Wu and A. Castellazzi, "Temperature adaptive driving of power semiconductor devices," 2010 IEEE International Symposium on Industrial Electronics, Bari, 2010, pp. 1110-1114.

[15] A. Soldati, F. Dossena, G. Pietrini, D. Barater, C. Concari and F. Iannuzzo, "Thermal stress mitigation by Active Thermal Control: Architectures, models and specific hardware," 2017 IEEE Energy Conversion Congress and Exposition (ECCE), Cincinnati, OH, 2017.

[16] J. Ewanchuk, J. Brandelero and S. Mollov, "Improving the die utilization and lifetime in a multi-die SiC power module by means of integrated per-die gate buffers," 2017 29th International Symposium on Power Semiconductor Devices and IC's (ISPSD), Sapporo, 2017, pp. 439-442.

[17] J. Ewanchuk, J. Brandelero and S. Mollov, "Lifetime extension of a multi-die SiC power module using selective gate driving

with temperature feedforward compensation," 2017 IEEE Energy Conversion Congress and Exposition (ECCE), Cincinnati, OH.
[18] N. Baker, S. Munk-Nielsen, F. Iannuzzo and M. Liserre, "IGBT Junction Temperature Measurement via Peak Gate Current," in IEEE Transactions on Power Electronics, vol. 31, no. 5, pp. 3784-3793, May 2016.
[19] N. Baker, L. Dupont, S. Munk-Nielsen, F. Iannuzzo and M. Liserre, "IR Camera Validation of IGBT Junction Temperature Measurement via Peak Gate Current," in IEEE Transactions on Power Electronics, vol. 32, no. 4, pp. 3099-3111, April 2017.
[20] J. Brandelero, J. Ewanchuk, S. Mollov, “On-line Virtual Junction Temperature Measurement via DC Gate Current Injection” 2018 International Conference on Integrated Power Electronic Systems (CIPS), Stuttgart, Germany, 2018

