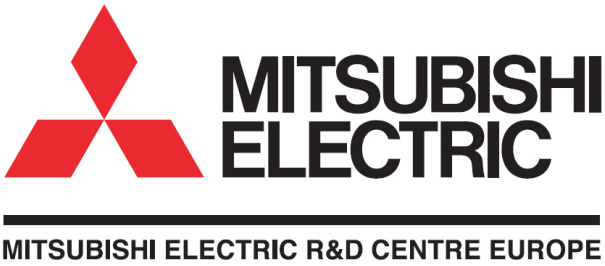

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Indirect On-State Voltage Estimation Using a Voltage Sensitive Electrical Parameter through the Gate Driver

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Abstract

Knowing the SOH (state of health) of a system is critical to organize an effective maintenance program to reduce cost and to prevent spontaneous failures of a power system. In this paper, an indirect method for estimating the on-state voltage in a multichip power module is presented. This method is based on the variation of the input capacitance and does not require any connection to the power terminals of the power module. The on-line developed method is described and implemented within the gate driver circuitry. Due to the temperature sensitivity of the gate-emitter voltage measurement, the same circuit also is used to determine the junction temperature of the semiconductor. The experimental results obtained during a calibration phase are shown and the feasibility of the presented technique for SOH estimation is discussed.

1. Introduction

In applications, such as traction systems or in wind energy generation systems, the total cost of a product is not fixed by its initial price. Total Cost Ownership (TCO) and Life Cycle Cost (LCC) are analysis methods developed to estimate the life cycle cost of a product by taking into account the purchase cost, taxes, maintenance and disposal cost. Trains are a great example where TCO or the LCC are used. Their long life cycle (up to 30 years) make maintenance related costs the most important quantity of the TCO. In the case analyzed in [1], the maintenance cost (preventive and corrective) represents 73% of the total cost of ownership; in fact, the purchase cost represents only the 1.5% of the total cost. Thus, reducing the maintenance cost of a product can have a significant impact on the total cost of that product.

Historically, the failures in power modules have typically been classified as random – thereby making it difficult to reduce the frequency of maintenance [2]. However, with advances in manufacturing quality, the component life-time has increased to a point where the wear-out of the part can be dominant. Thus, there is an opportunity to reduce the maintenance interventions by determining the state of health (SOH) of a component. In particular, a recent industrial survey for power converters indicates that the weakest components are the capacitors in a 30% of cases, followed by the PCB in 26% of the cases, and the power module in 21% of the cases [3]. Therefore having the SOH estimation of the power semiconductors may contribute to increasing the reliability of the system, to guide the maintenance phases, contributing for a preventive and fast maintenance programs, with lowered life cycle costs.

In power modules, the dominant wear-out failure modes are attributed to three main mechanisms: the reconstruction of the metallization, wire bond lift off, and delamination of the solder joints [4]. Owing to the increase in electrical resistance associated with the first two failure mechanisms, an opportunity exists to determine the SOH of the power device, i.e. by measuring the on-state voltage or the gate threshold voltage [5].

In this paper, an indirect on-state voltage estimation method is presented with the goal of measuring the power module deterioration for on-line SOH estimation. In the second section, the condition monitoring techniques including on-stage voltage measurement techniques are reviewed. In the third section, the indirect on-state voltage estimation method is described and the experimental results are shown. Finally a discussion on the applicability of this method to determine the state of health of a power module is held.

2. Condition Monitoring

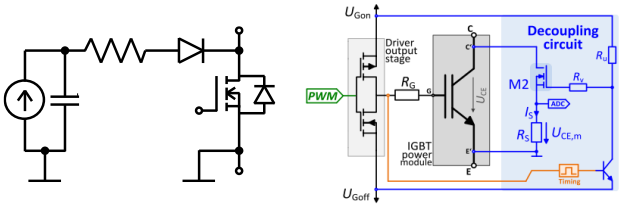
Three main aging mechanisms dominate the wear-out lifetime in a power module. The first aging mechanism is the reconstruction of the die metallization , caused by the mismatch in the

coefficient of thermal expansion (CTE) between the metallization and the silicon die during temperature cycles [4]. The second aging mechanism, wire bond lift off, is caused by crack propagation in the wire bond, which is driven by the thermo-mechanical loading. These wires, which conduct the load current of the power dies, experience a high degree of thermal loading due to their proximity to the surface of the power die, and the internal heating from the load current. Moreover, due to temperature gradients on the die surface, the distribution of current in the wire bonds can be non-homogeneous. Consequently, as both aging mechanisms degrade the electrical performance of the power module, an increase in on-state voltage can be observed due to aging. The last aging mechanism, the solder delamination, does not result in an increase in the electrical resistance in the load current path of the power module. However, as the thermo-mechanical fatigue causes cracks to propagate in the various solder interfaces, the thermal performance of the power module is degraded; thereby causing an increase in the junction temperature, *Tvj* , also applicable to the thermal interface further away from the power assembly.

An increase in the electrical resistance will impact the losses generated and consequently an increase of the junction temperature. In the same logic, an increase on the junction temperature will increase the voltage drop across the semiconductor working in the PTC region. Therefore, both *Tvj* and on-state voltage measurements are necessary to quantify and identify the current aging state of a power module.

2.1 On-state voltage measurement

The challenge for direct on-state voltage measurements is the dual requirement of withstanding high blocking voltages (kV range) and measure small voltages (mV range). One common technique uses a de-saturation protection circuit, as shown in Figure 1, with a diode in series with the measurement chain to block the high voltage (HV) when the main transistor is off. The main drawback of this technique is the compensation required of the diode drop voltage. Hence, several solutions have been investigated in literature to overcome the need to compensate this voltage drop, whether by thermally coupled HV diodes [6] or by the use of active or passive clamping circuits. In the latter case, the parasitic capacitance of the clamp diodes, the reverse recovery of these diodes, and the high resistance from the divider network typically result in slow response times. In contrast, active clamping circuits are fast in response but require expensive active components [7].



a) b)

Fig. 1. Direct on-state voltage measurement techniques a) direct measurement with series diode b) active clamping circuit [7]

In all the investigated techniques, direct measurements of the on-state voltage naturally results in a number of components connected to the high voltage terminals. Consequently, these components can reduce the robustness or performance of the whole system if they fail. Therefore there is a great interest for another method for V_{ce} measurement, i.e. by using the low power gate terminals.

2.2 Junction temperature measurement

The measurement of the junction temperature of a power semiconductor can be performed on-line via the use of temperature sensitive electrical parameters (TSEP). Among the TSEPs, the internal gate resistance is one of the most appealing parameter to be measured. In [8], the authors propose to measure the peak gate current as a TSEP-based method. An impedance measurement has been developed in [9] in order to estimate the junction temperature. Finally, the authors of [10] propose a gate current injection to measure the gate voltage variation as function of temperature.

In this paper, in order to complement the method of measuring the on-state voltage, the gate current injection technique for measuring the junction temperature is also employed. In this sense, the entire SOH estimation chain is employed by using the gate terminals only.

3. Indirect V_{ce} Estimation

3.1. Voltage sensitive electric parameter in IGBTs

An indirect on-state voltage estimation is made possible by measuring a voltage sensitive electrical parameter. In devices as IGBTs and

MOSFETs, the input capacitance Cin varies according to collector/emitter (source/drain) voltages. Therefore, the measurement of Cin by gate connection under certain conditions translates the voltage across the device.

As shown in [11], the input capacitance of a MOSFET, *Ciss*, varies with the gate-source voltage with a nonlinear relation with the applied gate voltage, *Vg*. Using a frequency response analyzer (ref. AP 300), the input capacitance (*Cin*) of a sample IGBT device is characterized for different gate voltage (*Vge*), and blocking voltages (*Vce*) as per Figure 2. Note that below -4V, the capacitance is nearly constant with *Vge*, and independent of *Vce*; thus, the *Tvj* estimation by the gate voltage measurement is independent of Vce in this region. With *Vge* between -4V and 0V, the input capacitance decreases with an augmentation in the *Vce* voltage. Therefore, a *Vce* estimation could be implemented with the *Cin* capacitance measurement for certain levels of a *Vge* bias voltage.

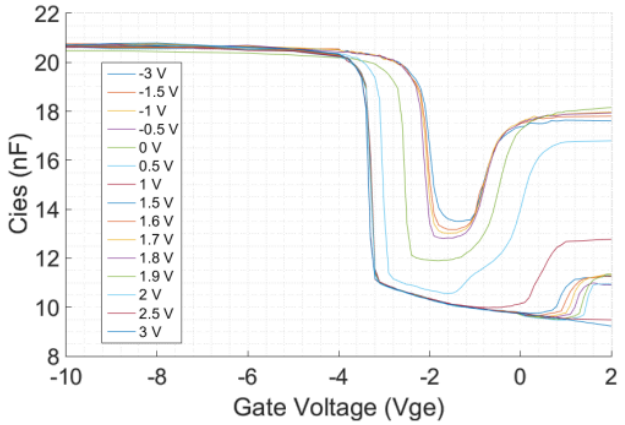


Fig. 2. Input capacitance evaluation for different V_{ge} at 22°C when varying V_{ce} bias

To measure the *Cin* capacitance, different methods can be used as the direct measurement with specific integrated circuits, e.g. capacitance to digital converters. In order to maximize the influence of the input capacitance, an integrator is built with a DC current injected through the gate–emitter. Given the current injected, the *Vge* voltage rises as function of the input capacitance, which is then dependent on the *Vce* voltage.

In Figure 3, the implementation of the gate driver with current source injection is shown. The transistor Q1 and Q2 drive the gate of the power device, 1 TOP, as a classical gate driver. During the current injection, the IGBT is in off-state and consequently Q2 is conducting, then the transistor Q3 is opened and the current flows through the IGBT gate. In this manner, the gate voltage is charged to an arbitrary level, depending on how long Q3 is open.

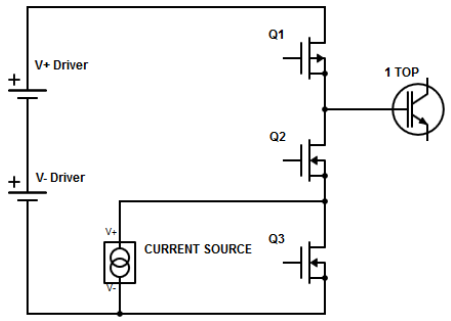


Fig. 3. Gate voltage evolution for different V_{ce} under constant current injection

The Figure 4 shows the impact of the input capacitance variation for different *Vce* bias when a current of 25mA is injected into the gate. Based on these results, an identification of the gate voltage at a given time, around sample 80, is selected to perform the *Vce* estimation.

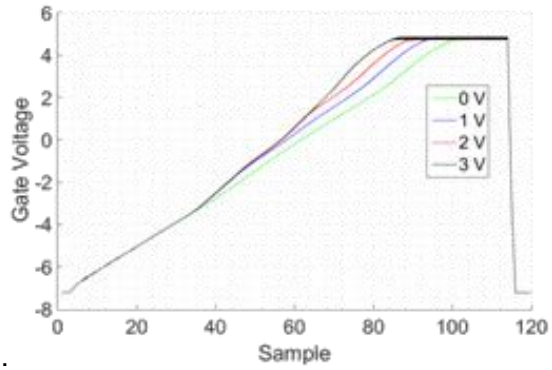


Fig. 4. Gate voltage time evolution for different V_{ce} under constant current injection.

3.2. On-line V_{ce} estimation methodology

In this paper, the online *Vce* estimation method employed uses a high current power module, composed of parallel dies, as shown in Figure 5. The power module has the characteristic of having per-gate pad connection. As a brief summary of the operation for the proposed technique, when the N parallel dies are conducting (in black), one die is turned off (in gray), and thus, each remaining die conducts 1+1/(N-1) fraction of the operational current. As the measurement time is very short, around 5µs as shown in Figure 4, only a small overheating is generated on the conducting dies. At this time, the gate of the stopped die is charged with a constant current to

estimate the *Vce* imposed by the all other parallel dies conducting. In order to reconstruct the individual *Vce*, the die which is turned off is shifted N times. In this manner, as the on-state voltage of each die can be measured, the level of degradation in each die can be hypothetically inferred.

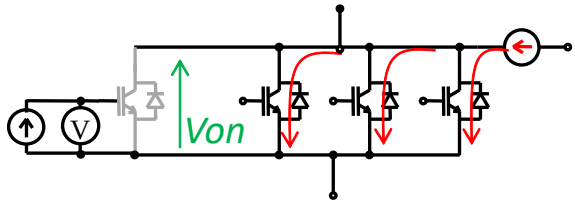


Fig. 5. One switch of a multi-die power module, in black, the dies on on-state; in gray, the IGBT enabling the on-state measurement of the on-state des

3.3. Elements for a precision-based design

The indirect on-state voltage measurement circuitry has two main components to be dimensioned: the current source, and the ADC. The value of 25mA has been chosen for the current source to allow significant charge in the gate in a small period of time (some microseconds), enabling its use in a switch-mode application. The precision of the current source output is an important parameter concerning the precision of *Vce* estimation. As it can be observed in the equation (1), a given current error, ∂I_{error}, will cause a V_{ce} estimation error, ∂V_{ce}, which will be amplified by the integration time *t*. Where *Ceq* is the equivalent input capacitance and $\Delta Vce/\Delta Vge$ is the sensitivity of the estimation.

$$\partial V_{ce} = t \cdot \frac{\partial I_{error}}{C_{eq}} \cdot \frac{\Delta Vce}{\Delta Vge} \qquad (1)$$

In a similar way the error caused by time quantification, ∂t_{error}, of the ADC can be calculated and a proper timer jitter selected:

$$\partial V_{ce} = I \cdot \frac{\partial t_{error}}{C_{eq}} \cdot \frac{\Delta Vce}{\Delta Vge} \qquad (2)$$

Finally, the total error include the current, timing and ADC ENOB (Effective Number Of Bits) as per (3).

$$\partial V_{ce} = \left(t \cdot \frac{\partial I_{error}}{C_{eq}} + I \cdot \frac{\partial t_{error}}{C_{eq}} + \frac{V_{ADC}^{max}}{2^{ENOB}} \right) \cdot \frac{\Delta Vce}{\Delta Vge} \qquad (3)$$

Taking into account that an average sensitivity about 0.4 $V_{ge}/V_{ce,}$as per Figure 7, the acquisition circuit can be fully dimensioned. In this paper, the current source is composed of a voltage source, ref. ADR435, buffered by an operational amplifier, ref. OPA211, loading a resistance to fix the current value. In this arrangement, the total current error is measured as ±1μA, and the clock generator of the ADC was measured to have a 15ps time jitter. Finally, the selected ADC (AD7626) has 14 ENOB. Hence, the estimated total error due to the selected measurement chain is approximately ±4 mV, in the worst case.

4. Experimental Results

As the V_{ce} estimation technique is based on an measurement of another voltage, a calibration procedure is needed. For this aim, a passive calibration was selected due to its inherent simplicity.

The V_{ce} is imposed by an external voltage source and the devices are heated with a hot plate to verify the dependency of the estimation with the temperature. The procedure is controlled by a real-time platform, i.e. using LabVIEW. In order to not activate the devices during the calibration, which would impose a high current level for a given Vce, the semiconductors of Fig. 6 are driven with a positive voltage inferior to the threshold voltage.

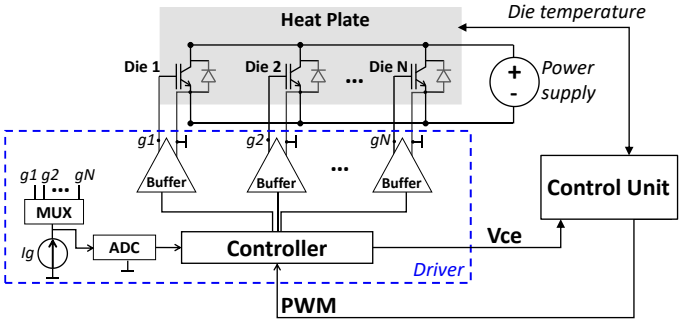


Fig. 6. Passive calibration platform schematic

The calibration procedure makes a sweep in the V_{ce} voltages in steps of 100mV between 0 V and 3.5 V, with each step applied for a duration of 6 seconds. In addition, a continuous sweep is done in the temperature of the components between 100°C and 40°C. Using a controlled hotplate, the temperature drop is set to 8ºC/hour, in order to have a good quantity of temperature points and ensure that a minimal thermal gradient exists in the thermocouple – power module measurement structure. Furthermore, before data collection, the temperature is maintained to 100ºC to ensure a good repartition of heat in the heat plate, thereby further ensuring a good approximation of the thermocouple temperature with the power device junction temperature.

In Figure 7, the results of the calibration are shown. The measurements shows a sensitivity of 0.4 V_{ge}/V_{ce} in the linear part of the curve, for a V_{ce} superior to 1.3V. With an increasing temperature at a given Vce, the corresponding gate voltage has only a slight variation for most of the investigated range.

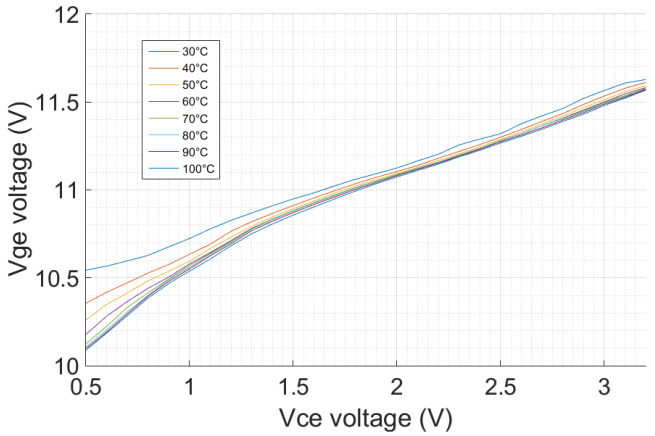


Fig. 7. Value of V_{ge} voltage (referenced to V-) at sample 80 for different V_{ce} with increasing temperatures

Furthermore, looking at the measured gate voltage as function of the temperature with increasing Vce, as per Figure 8, it can be seen that the temperature is mostly critical at low on-state voltage values. Thus, this phenomena may be compensated by the junction temperature measurement and a fitting algorithm.

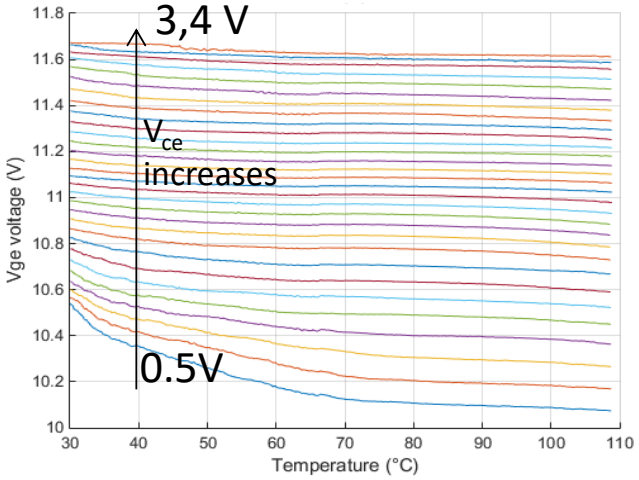


Fig. 8. Value of V_{ge} voltage (referenced to V-) at sample 80 for different temperatures with various applied Vce

The precision of the method was investigated by testing the device at a constant temperature for a long duration with V_{ce} voltage changed every 6 seconds. In the histogram of Figure 9, the V_{ce} dispersion can be observed during this test. Hence, it can be seen that a low dispersion of ±37.5mV is found throughout the range of applied voltages and temperatures.

Finally, in order to translate the V_{ge} measured voltage to the on-state voltage, a polynomial second degree fitting has been investigated to fit the experimental data -- resulting in a worst error of 250 mV, with a mean error around 100mV, as shown in Figure 10. Depending on the computational treatment capacity (FPGA or CPU) the accuracy might be improved using a lookup table or a polynomial 3rd order.

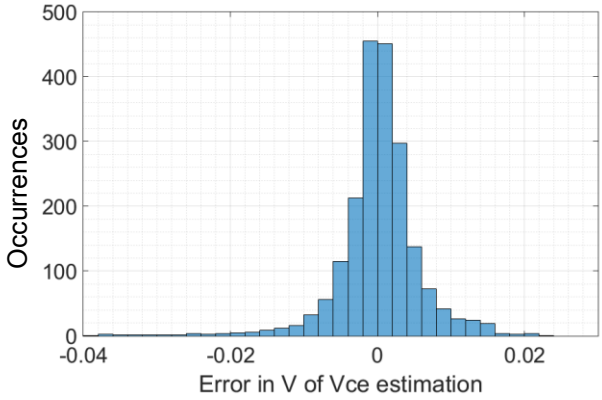


Fig. 9. Histogram of the error dispersion during precision tests

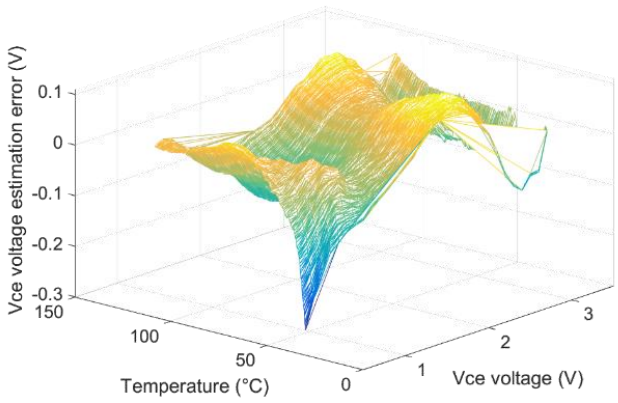


Fig. 10. Committed error with a 2nd degree polynomial fitting

5. Discussion

The damage-sensitive electrical parameters (DSEP) are often obtained by a direct measurement of the voltage quantities as the on-state voltage. The precision of this measurement is less important than the accuracy, given that each power module is monitored from their initial condition from a calibration step. In the case of the DSEP presented here, the initial value of *Vge* is to

be calibrated when under load current, which typically resulting in a on-state voltage higher than 1.3V. In this case, the linear evolution of the *Vge* with respect to *Vce* features a good sensitivity to the metallization and wire-bond deterioration. A current sensor may also be associated with the junction temperature and Vce estimation to better co-ordinate the damage estimation of the power module.

6. Conclusion

The use of a SOH indicator can reduce the total lifetime cost by preventing critical failures and allowing a just-in-time predictive maintenance. In power modules, the on-state voltage drop is one of the most important parameters to monitor as a damage sensitive parameter. In this paper, an indirect method to estimate this parameter is described. The greatest strength of this method consists in the insulation from the power paths, thus any measuring device is not directly connected to a high voltage connection.

The indirect estimation of the on-state voltage is based on the input capacitance value dependency. This capacitance is charged with a constant current and the voltage Vge is acquired. Thus, the on-state voltage of parallel devices may be estimated based on a calibration step. This methodology is fully compatible with the *Tj* estimation based on the internal gate resistance method presented in [10].

The results show a dependency of the Vce estimation with temperature in the range comprise between 0.5V and 1.3V. Above 1.3V, the Vge measurements are linear with the Vce voltage and quite independent within the power devices temperature.

As a future work, the test of this method in a power module in normal operation must be done to completely confirm the viability of this method.

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