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A PCB based package and 3D assembly for high power density converters

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***Abstract*— This paper presents a new power module suitable for wide band-gap device packaging. The module is a switching cell composed of a power stage, bypass capacitors, a bootstrap gate driver and an output inductor. The power stage is arranged in a 3D vertical structure. The stray loop inductance is extremely thus small due to a vertically placed ceramic capacitor. The module incorporates a gate driver and an output reactor using a molded compound material as a magnetic core. The paper shows prototype cross sections showing the component embedded in the printed circuit board (PCB) substrate, static electrical characterization of the chip and the switching performance of this package.**

Keywords—SiC MOSFET, PCB embedding, 3D power electronic, Power electronic packaging

I. INTRODUCTION

Wide band gap (WBG) devices are stated to be the future of power electronics. They present an opportunity for a higher power density at a minimized system cost. However, this can only be fulfilled by a package suiting their fast switching capabilities and permitting a good thermal management. Conducted and radiated electromagnetic (EM) noise are major challenges for these devices because of their fast transitions which lead to very high dV/dt. In addition, standard power module manufacturing process involves heterogeneous die interfacing techniques such as soldering and wire bonding that causes a poor manufacturing yield and low reliability of power modules.

Integrated power board (IPB) [1] packaging technology consist of embedding power devices into the multilayer structure of a printed circuit board (PCB). It is an attractive technology for WBG devices thanks to its lower package parasitic inductance [2] which allows a faster switching transitions and higher switching frequencies. This technology gives also the opportunity for a system level integration which reduces the number of interconnections for higher system reliability.

In Empower European project [1], a 500 W rating power module for Pedelec applications was demonstrated. The module uses sintered IMS substrate in order to improve the cooling of the module. In [2], Hoene et al. manufactured an ultra low inductance power module (down to 1.1 nH) using the PCB integration technologies. Kearney et al. [3] developed a PCB integrated power module which contains IGBT and diode switches. This paper shows clean switching waveforms of the module. It also shows good insulation and reliability test results. IPB technology offers also the possibility for more advanced packaging such as 3D power stage integration or heterogeneous integration. In [4], a 3D integration of the power module is done using the PCB technology. The module presents very low parasitic level of the switching loop and the gate control loop which allows a better parallelization of the power devices. Hou et al. showed in [5] a heterogeneously integrated power supply module where they integrated the dies in the PCB and assembled with a LTCC based inductor.

This paper presents a new package of a standalone switching cell that overcomes most of the challenges associated to the WBG devices. This covers the package thermal, electrical, EMI and manufacturing performances as well as the system level integration. The paper is organized in two major sections. The first shows the module structure and the module key features. The second, presents the characterizations of the module and discusses the obtained results. In the final section the paper is concluded.

II. MODULE PRESENTATION

A. Chip embedding in PCB

Chip embedding consists in introducing the power semiconductor chips in the multilayer structure of a PCB. The process can be described as follows. First, the power semiconductor chip is glued to a copper sheet. FR4 sheets are then cut to the size of the dies and stacked on the copper sheet. Another full FR4 sheet is used to cover the stack, thus, the dies. Finally, a full copper sheet is added on the top. The entire stack is laminated resulting in a solid assembly where the dies are held by the FR4 material and sandwiched between two copper sheets. A laser drilling process is used afterwards to expose the pads of the device for a copper plating process that connects the device pads to the copper conductor layers. The final step is an etching process in order to create the desired layout on the PCB. This first assembly, illustrated in figure 1, can be integrated in any standard PCB process afterwards to complete the desired circuit or module. Note that the pads of the semiconductor chips need to be copper finished in order to be compatible with the PCB copper plating bath.

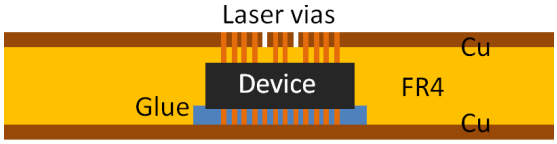

Figure 1: Illustration of an embedded semiconductor device in a PCB

B. Presentation of the core switching cell

A standalone switching cell is considered to have all the features needed to perform a power electronic switching function. Therefore, the module presented in this paper has the following parts (see figure 2):

- two power semiconductor switches arranged in a totem-pole topology
- bypass capacitors
- output inductor

- gate driving circuitry

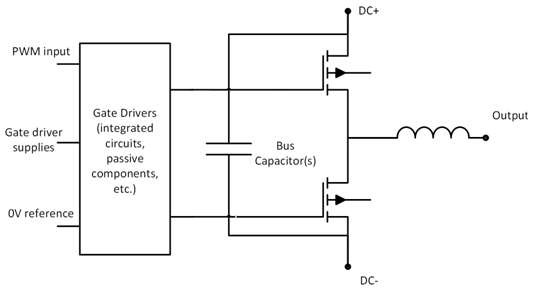

Figure 2: Schematic of the switching cell

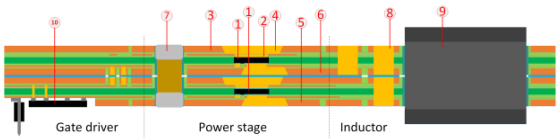

Figure 3: Sketch of the designed module

This power switching cell is implemented in a laminate substrate. An artistic sketch of this implementation is shown in figure 3. As seen in the latter figure, the module is divided in three parts, a gate driver, a power stage and a planar inductor. The module is made of four thick copper layers (400 µm) and four thin copper layers (35 µm). The thin copper layers are required to connect to the die pads. The thick copper layers are increasing the current carrying capabilities and improving the thermal spreading. The power stage is made of two SiC devices labeled (1). They are assembled in a 3D configuration. The low-side switch is located in the bottom side of the PCB and the high-side switch is located on the top side of the PCB. The SiC devices are connected with micro vias (2) to the thin copper layers. The thick and thin copper layers are connected by bigger size mechanical vias (4). In this configuration the power devices (1) are connected between the top copper layer (3) as DC- and the bottom copper layer (5) as DC+. The output of the switching cell (middle point) is composed of two thick copper layers labeled (6) on figure 3. Very close to the 3D power stage there are vertical ceramic capacitors (X7R 1kV) named (7) on figure 3 which are assembled between the bottom DC+ and the top DC-. On the right hand side of the module is shown an inductor where the windings are made by the copper layers of the module. Mechanical vias (8) are used to connect the turns on different layers of the module stack. The magnetic material (9) is a low temperature epoxy based compound material which is molded around the PCB windings. This low temperature process does not require any sintering step and is therefore compatible with PCB manufacturing process. On the left-hand side of the module, a gate driving circuit is assembled. It is a bootstrap circuit which allows us to reduce the size of the gate driver real estate. The gate driver circuit contains a gate driver Integrated circuit, a bootstrap diode and a few passive components (capacitors and resistors), as well as a pin head connector for controlling the module. These fine pitch components are soldered on one thin copper layer of the PCB (35 µm) which is exposed by a routing PCB process.

This module has several great features that give it superior characteristics for a power electronic switching cell. The 3D configuration of the chips combined with the vertical bypass capacitors in the vicinity of the switching devices induce a very small parasitic loop inductance for a power stage. This feature is critical in case of fast switching devices such as vertical SiC MOSFETs. Thanks to the obtained very low parasitic inductance, Voltage overshoot during turn-off and post-transition ringing will be minimized which reduces significantly the conducted electromagnetic (EM) noise emissions. Furthermore, the switching node which is located between the two devices is shielded between the DC- and DC+ outer copper layers. This configuration reduce significantly the radiated noise emissions that could be an issue in the case of fast switching devices. The complete module has four copper layers of 400 µm thickness. This high amount of copper close to the chip creates a superior current carrying capability in addition to a better heat spreading leading to a better thermal performance. Moreover, as oppose to standard DBC technology, the versatility of the PCB process allow us to combine thick copper layer for a high current and power capabilities and thin copper ones for the fine pitches and lower power circuitry ; here the gate driving circuit. Such feature allows us to reduce the number of connectors and soldering steps limiting the number of manufacturing processes and increases the reliability. This increases the manufacturing yield, and thus, reduces the cost of the module. Cost by the unit is also reduced by the parallel nature of the manufacturing of a PCB substrate. Finally, the low temperature process used for the inductor gives another opportunity for cost reduction as it has a temperature compatible with the PCB process, it can be done on the same production chain.

C. *Cooling of the power module*

A multifunctional busbar is used in order to make a converter assembly out of the module presented earlier. This busbar serves two purposes. First, it is used as the electrical connection of the converter to application power source. Second, it is used to cool down the power devices by circulating a fluid in the cooling channels. Thus, two busbars assembled on the top and bottom sides of the module in order to provide the DC+ and DC- bus connections, also, to extract the heat from the top and bottom switches. This assembly is then, as showed in figure 4, a double sided cooling of a 3D configuration power stage.

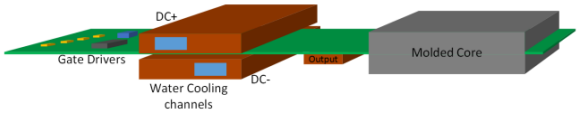

Figure 4: Cooled busbars for module cooling and supply connection

III. Manufacturing Analysis and Characterization Results

This module described in the upper section has been manufactured in a standard PCB manufacturing line. No special process steps or equipments are needed. The following subsections shows the manufacturing output and the electrical characterization.

A. *Manufacturing output*

Two SiC copper metalized MOSFETs were embedded in the PCB substrate. The compound magnetic core is molded around the inductor turns. The bypass capacitors as well as the gate driver devices are assembled by a standard reflow process. A photograph of the module is showed in figure 5.

Multiple cross and flat sections of the manufactured module were done and two examples are showed in figure 5.

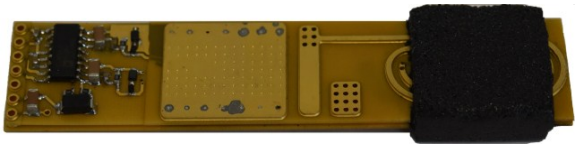

Figure 5: Picture of the manufactured module

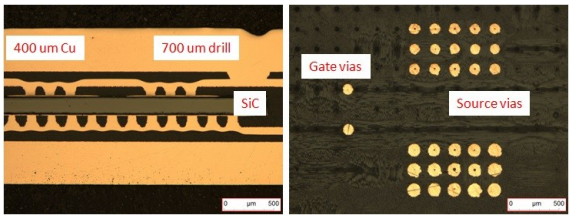

Figure 6: (left) Cross section and (right) flat section of the module

In figure 5, one can see the gate driver circuit on the left side of the module, the power stage with small dimples created by the vias in the center of the module and the molded core and windings of the output inductor on the right side.

As it can be seen on the cross-section image of figure 6, the SiC power device is successfully embedded into the PCB substrate. No sign of damage have been reported during the analysis. On the upper part of this picture, it can be seen two sets of three microvias connecting the source pads of the MOSFET and in the lower part, it can be seen one set of twelve microvias connecting the drain pad of the MOSFET. On the upper right corner, we can see one 400 µm copper layer connected to the 35 µm copper layer with a 700 µm diameter mechanical via. On the flat section view of figure 6 it can be seen the microvias connecting the top side gate and source pads of the MOSFET.

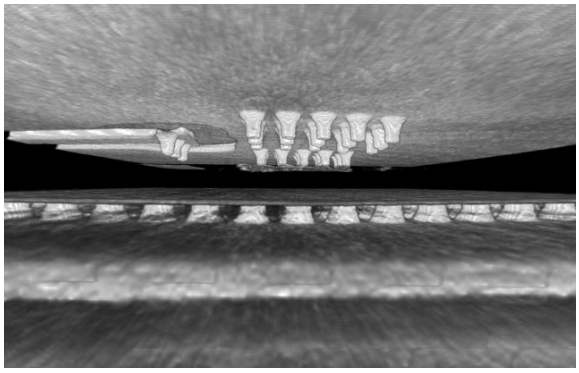

Figure 7: 3D x-ray tomography of the embedded device

Figure 7, shows a 3D x-ray tomography of an embedding device. One can see the copper pillars which correspond to the microvias touching the semiconductor die. On the bottom side we can see the drain vias and the die metallization. On the top side we can see the gate and source vias. Note that the die is invisible in this configuration.

Figure 8 shows a cross section of the 3D power stage after the assembly of the decoupling ceramic capacitors. The package size of these components is chosen to fit the module total thickness. The capacitors are placed in back-drilled cavities before assembly of the two sub-modules. Prior to the capacitors placement, solder paste is applied on the bottom of the cavities. The electrical connection will be realized at the same time as the gate driving circuitry during the reflow process. On figure 8, it can be seen the switching loop of the power stage which is located between the capacitor and the power devices. The loop size is reduced to the minimum leading to a stray inductance in the picoHenry range.

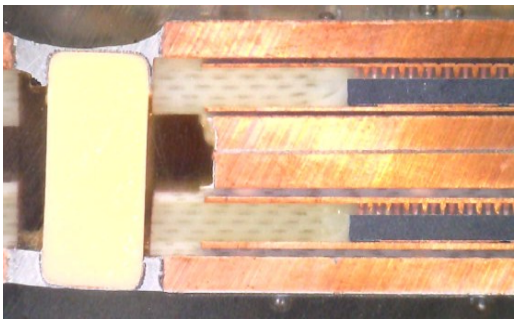

Figure 8: 3D power stage with vertical capacitor assembly

B. Static electrical characterization

The electric characterization of the devices is done using a curve tracer, in order to evaluate the PCB embedding technology compared to the standard packaging. The threshold voltage V_{th}, the leakage current $I_{DS\text{-}off}$ and the on state resistance R_{on} are measured. The results are shown in figure 8, 9 and 10 respectively.

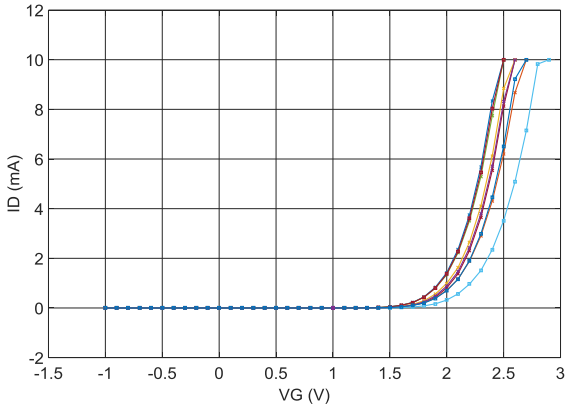

Figure 8: V_{th} measurement of the embedded devices

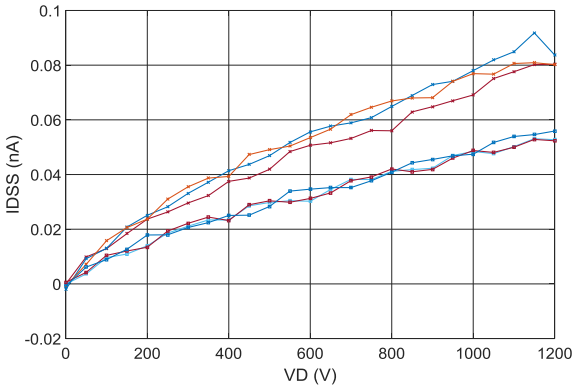

Figure 9: Leakage current of the embedded devices

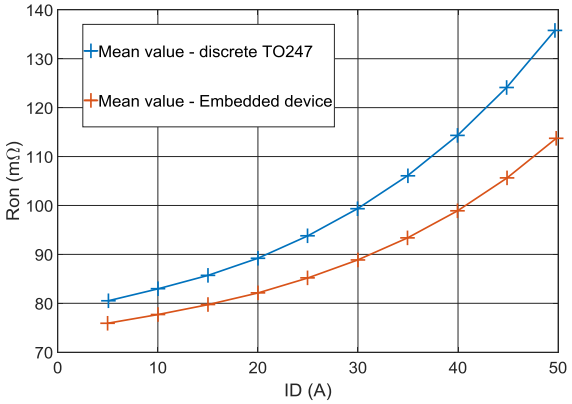

Figure 10: R_{On} measurement of TO247 and the embedded package

Reference values are either taken from the component datasheet or extract from a standard TO-247 package of the same device. The threshold voltage is measured in the same conditions as the datasheet (V_D = 10 V ; I_D = 5 mA ; 25 ^{0}C). It can be seen from figure 9 that V_{th} is equal in approximation to 2.3 V which is consistent with the value provided in the datasheet. In figure 9, the leakage current is below 0.1 nA for a drain voltage up to 1200 V and a 0 V gate voltage. These values are within the range given in the device datasheet.

In figure 10, the On-resistance of the embedded device in terms of the drain current is compared to the same device enclosed in a standard TO247 package. Note that, the curves obtained in both cases (embedded and TO247) are an average value after measuring more than 6 devices every time. It can be clearly seen that the embedded device package presents lower package resistance compared to the TO247. The difference is 5 mΩ at 5 A, 11 mΩ at 30 A and 22 mΩ at 50 A. The difference is increasing with the drain current which we attribute to the self- heating effect of the device at higher current levels.

Based on the cross and flat section presented in the earlier subsection and the static electrical characterization, we can deduce that the power devices are successfully embedded in the PCB substrate.

C. *Dynamic test*

The next characterization step is to perform switching test of the module. Thus, the module is assembled with the liquid cooled busbar for supply and the gate driver circuit is fed with the classical two-pulse method, signals being generated by a digital signal processor (DSP). The switching waveforms of the double pulse test can be seen in figures 11 and 12.

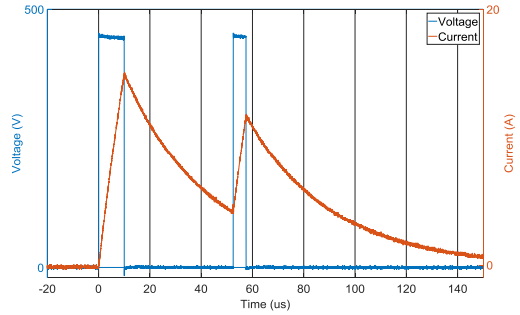

Figure 11: Double pulse test of the embedded module

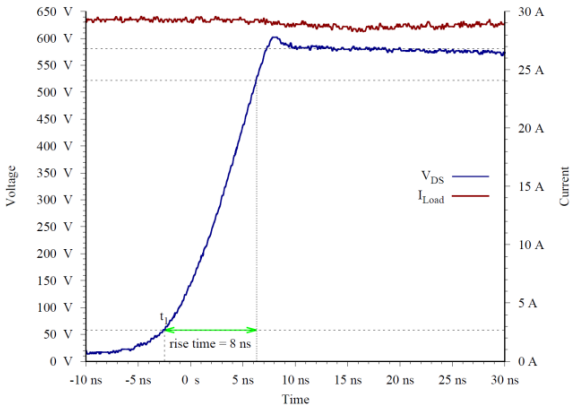

Figure 12: Switching transition of the embedded module

In figure 11, the drain to source voltage of the bottom switch and the load current are shown. No current sensor can be added in the switching cell for visualizing the device current, partially because of the vertical structure but mainly because inserting current sensor will drastically degrade the remarkable stray inductance. The bus voltage is 450 V and the peak current during the second turn-off is 15 A. The drain to source voltage, in blue, presents total absence of ringing or overshoot during both «On" and "Off" transitions. The second "On" transition is switching with a load current of approximately 5 A which proves the normal operation of the MOSFET body diode since the dead time is fixed to 50 ns. Note that no external gate resistance has been added and the only resistance in the gate circuit is the internal chip resistance of 4.6 Ω.

Figure 12 shows another turn-off transition with a bus voltage of 600 V and a load current of 30 A. As can be seen the switch time is 8 ns which means this module is capable of switching at a rate of 58 kV/µs without any ringing and a very low voltage overshoot. This proves the extreme low parasitic inductance of the switching loop achieved with this module thanks to the 3D power stage and vertical capacitor configuration.

IV. Conclusion

This paper presents a standalone switching module made with the chip embedding in PCB technology. This technology gives a very high flexibility that allows us to add a gate driver, a bypass capacitor and an output inductor on the same substrate. Cross and flat sectioning of the module confirmed a successful manufacturing process which was confirmed again with static electric test. Due to the proximity of the gate driving circuit, the gate loop is very small. It has

been shown also that the switching loop is very small which allows us to obtain an extremely small parasitic inductance. Thus, the module presents extreme switching capabilities thanks to its extremely small loop inductance. A switching transition of 58 kV/µs with a total absence of ringing is achieved.

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