IEEE Transactions on Power Electronics (Volume: 36, Issue: 1, Jan. 2021)

DOI: 10.1109/TPEL.2020.3002188

Selective Gate Driving in Intelligent Power Modules

Julio Brandelero

Jeffrey Ewanchuk

Stefan Mollov

Selective Gate Driving in Intelligent Power Modules

Julio Brandelero, *Member, IEEE*, Jeffrey Ewanchuk, *Member, IEEE* and Stefan Mollov, *Member, IEEE*

***Abstract*- Due to practical limitations in the manufacturing of power semiconductor dies, high power modules are composed of several dies in parallel in order to meet the desired load current requirements. With careful attention to the design, modern IGBT-based power modules feature relatively balanced current distribution amongst the parallel dies. However, owing to the increased switching speeds of wide bandgap devices, i.e. SiC, it is challenging to design the package to achieve both low-loss and balanced operation. In this paper, a technique is proposed where the individual dies in a multi-die power module can be selectively driven by a closely integrated gate buffer. Amongst the benefits achieved by selectively driving the die gates, a profiling of the power loss within the intelligent power module is enabled. Furthermore, a practical technique to estimate the individual die temperatures is presented, and using the same method, the on-state voltage of the power module during load current conduction can be estimated. Lastly, it is experimentally demonstrated that the combination of individual junction temperature estimation and the selective gate driving can be used to increase the power density of the power module by better utilizing the component dies.**

***Index Terms*—Power semiconductor devices, Multichip modules, Gate driver, Temperature balance, SiC devices, Thermal balance, Driver circuits, Temperature measurement, Temperature control, Voltage measurement**

I. INTRODUCTION

THE rapid development of power electronics has enabled an increasing electrification of our every-day lives. However, further adoption of power electronics in harsh environments and critical applications, amongst which energy generation and distribution and aerospace, require a significant increase in their reliability in order to be considered for their large-scale adoption [1]. Thus, a significant amount of research effort has been dedicated to understanding how to improve the availability of power electronic converters, for example with the Highly Efficient and Reliable smart Transformer (HEART) project for distribution systems [2], or the Reliable Power Electronics (ReliPE) project for high voltage transmission systems [3].

On another axis, wide bandgap power semiconductors, such as SiC or GaN are maturing and have an important role in improving the power density of power electronic converters. Due to the high dv/dt and di/dt from these power devices, and particularly related to the electrical parasitic elements from the power device packaging, the gate driver design is critical to exploiting the maximum performance [4]. One emerging trend, especially relevant for GaN power devices, is to integrate the gate driver close to the power semiconductor switch, i.e. as shown by GaN Systems [5], and Navitas Semiconductor [6]. Moreover, the limitation on the current capabilities of the devices lead to chip parallelization, as shown in Fig. 1 with advanced packaging structures and symmetrical layouts in order to achieve high power [7 - 9]. An intelligent power module approach with parallel dies that incorporates gate buffers tightly coupled to each individual die is presented in this paper. This allows for a reduction in the switching losses by reducing the total gate loop inductance, minimizes the interaction with the load current through the emitter/source inductance during the switching and helps to distribute the current during the transition time [5-6], [10-11].

Active gate driving concepts with more intelligence integrated in the gate driver are proposed to overcome some limitations from the power device packaging, as shown recently with a multi-level active gate driver [12], and active gate drivers with controlled output voltages [13-15]. A further development in integrated gate drivers is the inclusion of condition monitoring technologies to reduce the lifecycle cost of the converter with just-in-time maintenance [16-21]. In particular, these gate drivers incorporate on-board analog-to-digital converters (ADCs), and computational intelligence to estimate the approximate state of health of the converter, i.e. by measuring the on-state voltage [17], estimating the junction temperature [19] or by estimating the thermal resistance [20-21]. A technique using only the gate terminals that allows for the estimation of the individual junction temperatures of each die is presented in this paper. The technique is then extended to allow for measuring of the on-state voltage of the power module during operation [38], and thereby enabling certain condition monitoring functions.

While current balancing between power modules is extensively treated [7, 21-27], it is recognized [28] that the

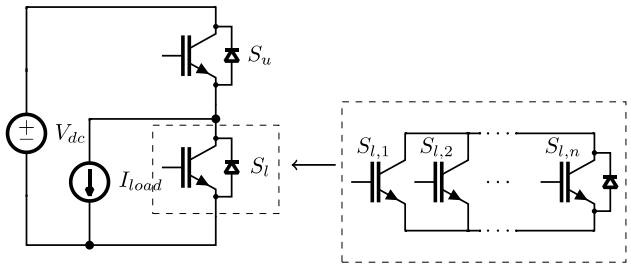


Fig. 1. Half bridge topology in a power module with *N* dies per switch.

J. Brandelero is with the Mitsubishi Electric Center Europe, Rennes, France (e-mail: j.brandelero@fr.merce.mee.com).

J. Ewanchuk was with Mitsubishi Electric Center Europe, Rennes, France during this work. He is now with the Raytheon Technologies Research Center, East Hartford, CT 06108, USA (email: ewanchje@rtx.com).

S. Mollov is with the Mitsubishi Electric Center Europe, Rennes, France (e-mail: s.mollov @fr.merce.mee.com).

approach does not address the actual stressor – the dies' junction temperature. In addition, the implementation of inter-die static and dynamic current equalization is impractical, due to the extreme requirements on the current sensors: large bandwidth, noise immunity, harsh environment, complexity of integration and lossless operation. In this paper we propose a method of selectively driving the gate of each die, that uses a closed-loop algorithm for steering the losses and thus equalize the die temperatures.

The first section of this paper discusses the benefits and the drawbacks when using smaller and numerous parallel dies. The second section presents the proposed approach to better utilize and monitor the paralleled dies in a power module thanks to the per-die driven gates. The junction temperature and the on-state voltage measurement techniques, enabled by this approach, are also presented in Section III. The fourth section presents the techniques to redistribute the thermal stress amongst the parallel dies. Finally, it is experimentally shown in a SiC MOSFET prototype and in a Si IGBT prototype that the power module can handle up to 25% more load current by internally balancing the die temperatures through the better utilization of the dies within the power module.

II. Multi-Die limitations in High Current Power Modules

Multi-die power modules are commonly used to commutate large currents. However, in terms of cost, it is not obvious why less numerous, larger dies might be preferred over smaller, more numerous dies. This section reviews the benefits and drawbacks of a multi-die power modules.

A. Benefits of Using Smaller Dies

While the general trend of high power modules is to increase the individual die size, and therefore reduce the number of parallel dies in a power module, it is not a general rule that larger dies are better in operation than smaller, more numerous dies. In terms of cost and thermal spreading, smaller, more numerous dies have a distinct advantage over their larger equivalent dies.

As a motivating example, an arbitrary 6" circular wafer is considered, where the composite dies on the wafer have a square shape with an increasing die width in mm. Given the shape of the wafer, and an assumed thickness of wafer saw, a number of dies can be obtained from the wafer, as shown in Fig. 2 (a). As the die size increases, the number of dies obtained from a single wafer eventually decreases. However, with a standard defect density of 0.1 defects/cm^2, the total number of dies is dramatically reduced compared to that of the zero defect density case. Therefore, as the final cost of the semiconductor component is related to the yield, it is clear that smaller devices can result in lower manufacturing costs.

Furthermore, smaller dies can better utilize thermal spreading to achieve lower thermal gradients when compared to larger dies. As shown in Fig. 2 (b), two synthetic designs of a power module with a traditional package were analyzed using a Finite Element Method, assuming a fixed loss density of 20W/cm^2.

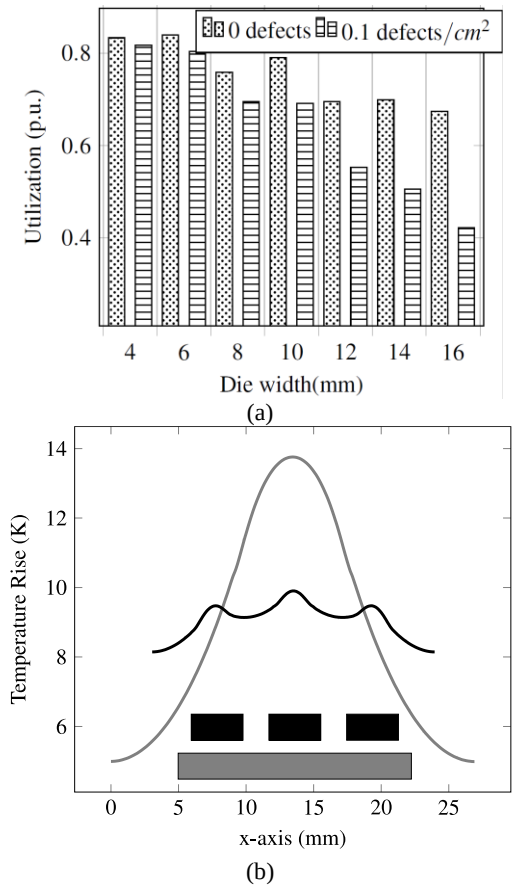


Fig. 2. Benefits using smaller dies (a) yield of a wafer as a function of die width (mm) for two defect densities, and (b) temperature rise across the linear distance of a single die (gray) against three dies with a similar total area (black)

The first design employs a single die to meet the design target, and exhibited a maximum thermal gradient of 14K across the surface of the die. Alternatively, a design assuming three parallel smaller dies (5mm vs 16mm) featured a maximum of 10K across each surface of the individual dies. While the average temperature of each solution was identical, the temperature distribution of the multi-die solution was more even, and the peak temperatures were smaller. Therefore, smaller dies can simultaneously result in lower manufacturing costs, and lower temperature gradients on the surfaces of the individual components.

B. Drawbacks with Smaller and More Numerous Parallel Dies

Unfortunately, there are a number of drawbacks to using more numerous parallel dies to achieve a given load current rating in a power module. Firstly, the design of the power module must accommodate the electrical and thermal connection to the external world to each individual component.

Owing to the differences in the power loop impedance and the driving loop impedance, the current distribution between the parallel devices is not ideal [22-24]. Layout techniques and guidelines to avoid derating on power modules concentrate the effort in reducing the parasitic impedances and having it symmetric [29-32]. Paralleling half-bridges instead of dies were

shown [7, 34] to improve current sharing. While the current balancing issues can be reduced by using a common kelvin connection, the impact of a non-ideal electrical layout within the power module on the distribution of switching losses can be drastic [34]. Furthermore, as the thermal path cannot be guaranteed to be the same for all the dies, the temperature imbalance occurs even for a same power dissipation in each parallel die.

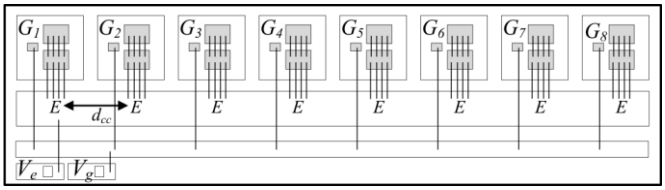
As a motivating example, 8 parallel dies form an equivalent switch and are connected as shown in Fig. 3, with a spacing of $d_{cc} = 1.8\,cm$, a bus-bar inductance of $5\,nH/cm$, and a bond wire inductance of $10\,nH$. The incremental source/emitter inductance in this example follows (1). In total, the source/emitter path difference differs by up to $9\,nH$, with a total source/emitter inductance of $19\,nH$ from the distance of the gate pad to the last die in the parallel set. This total source/emitter inductance impacts the switching losses by modifying the applied gate voltage, $v_{ge}(t)$ as shown in (2), as detailed in [10] and based on the analytical work presented in [35].

$$\Delta L_s = n \cdot L_g \cdot d_{cc} \tag{1}$$

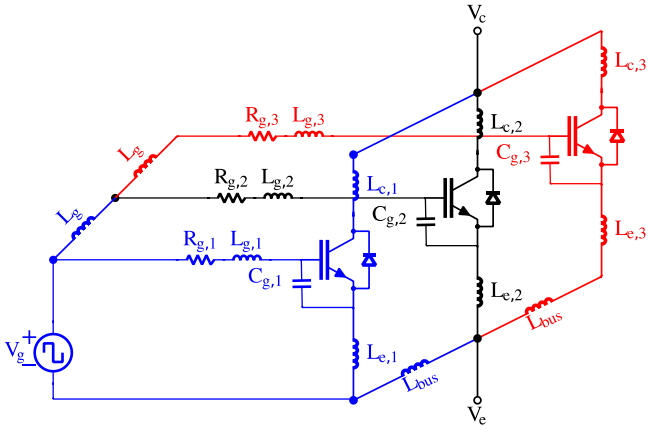
$$E_{loss} \propto L_s g_{fs} \exp\left(-\frac{t}{R_g C_{iss} + L_s g_{fs}}\right) \tag{2}$$

where $g_{fs}$is the transconductance of the MOSFET.

Given then a common emitter/source inductance design, the distribution of switching losses between the furthest MOSFET die to the nearest MOSFET die can be severe, though increasing the gate resistance can mitigate this unbalance to some extent, as shown in Fig. 4 (a). The relative increase of switching losses from one die in Fig. 3 (a) to the first die, with the smaller gate

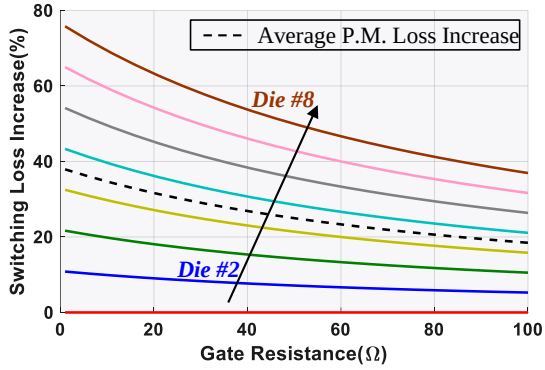


(a)

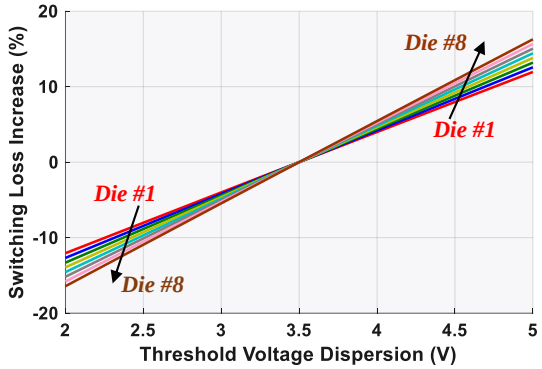


(b)

Fig. 3. Gate driving multi dies module (a) Substrate connection with a common emitter/source layout for 8 parallel dies (b) Electrical schematic of the parasitic network of three parallel dies in common emitter



(a)



(b)

Fig. 4. Turn-on switching losses across 8 parallel dies (a) with increasing gate resistance, and (b) increasing threshold voltage dispersion

driver path, is considered with only the turn-on transition and neglecting the reverse recovery of the inverse diode. In this case, a low gate resistance implies a relative average difference of nearly 1.4 times the first die along the substrate in Fig. 3 (a).

While topological compromises between thermal and parasitic requirements can be found, the semiconductor device parameters that vary due to the manufacturing also impact this current unbalance [24, 34]. In particular, the threshold voltage of each power device can differ, causing asymmetric switching losses [34] as shown in Fig. 4 (b). Using the same assumptions under the switching conditions as in Fig. 4 (a), with 3.5V as the reference threshold voltage, the impact of increasing the threshold voltage across the neighboring 7 dies is shown in Fig. 4 (b) for the substrate layout of Fig. 3 (a). Thus in this example, a threshold voltage variation of 0.5V can impact the turn-on switching losses by over 10% in the furthest die. Consequently, as the threshold voltage cannot be compensated by the design of the electrical routing of the power module, the parallel dies can be selected by matching their electrical characteristics [37] – a step which naturally comes associated with a cost.

III. Selective Gate Driving of Power Modules

In this paper, a solution to take advantage of the cost benefits of smaller, more numerous dies, while mitigating the adverse impact of the packaging and parameter mismatching is proposed, termed ‘selective gate driving’, wherein each power die is individually driven. The substrate requires a modification in order to enable the individual access to each emitter/source

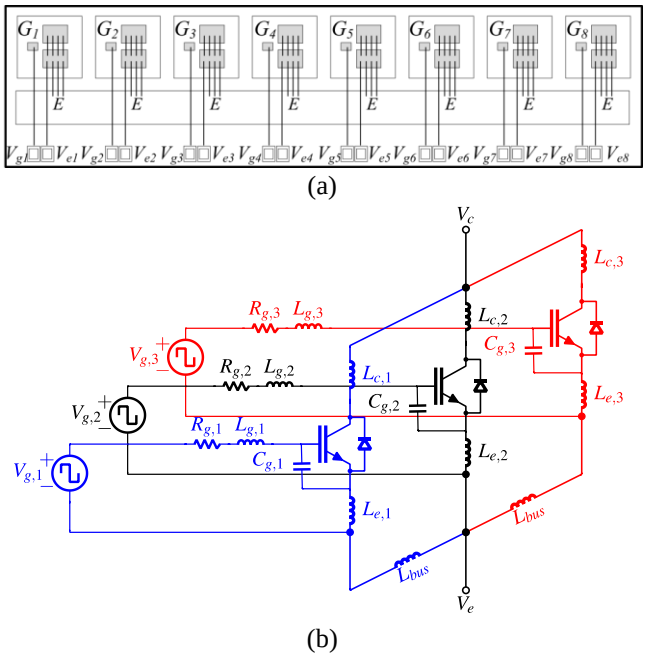


Fig. 5. Individual Gate drive of multi dies module (a) layout of the substrate and (b) Individual gate driven equivalent electrical schematic

pad, as shown in Fig. 5 (a), similar to that required for Kelvin emitter/source access. Advantageously, the selective driving reduces the switching losses, increases the controllability and permits the per-die condition monitoring functions.

In this case, the parallel dies are on a common electrical reference and the addition of individual gate buffers, as shown in Fig. 6, does not require costly individual power supplies. This solution is designed to be compatible with the concept of intelligent power modules, where the gate driver and power dies are integrated within the power module structure. Another advantage of the selective gate driving is the increased controllability, whereby the dies can be delayed relative to each other, or enabled/disabled during a switching commutation. This allows the FPGA/CPLD to manipulate the driving pattern to each die individually, without affecting the output voltage at the terminals of the power module - this will be discussed in section IV

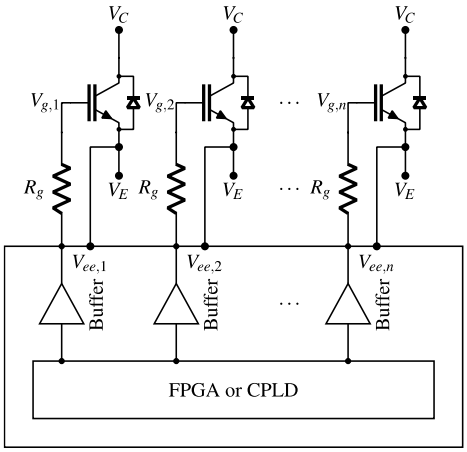


Fig. 6. Selective Gate Driven for intelligent Power Module: the integration of the individual gate buffers and coordinating control logic on the same emitter potential.

A. *Reduced Switching Losses and Increased Controllability*

The selective gate driving approach inherently shares a decoupled driving path from the neighboring dies, Fig. 5 (b). Hence, it not only enables optimizing the power layout as proposed in [7] for improved commutation, but also allows for reduced switching losses of the dies impacted by the ΔL_s . This is attributed to the reduced interaction between parallel sets of power devices [10]. As a consequence, selective gate driving permits a power module loss saving by the amount indicated by the curve "average loss increase" in Fig. 4 (a).

Taking for example the prototype of Fig. 15, the measured switching energies of SiC MOSFETs are given in Table I for the single gate access and with the selective gate driving approach. As expected from Fig. 4 (a), the results show an average reduction of more than 30% on the turn-on losses during the operation of the power converter.

TABLE I
SWITCHING ENERGY
VDC = 500V, IDC = 40A, PWM = 200 KHZ, Rg = 12Ω

Die Pos.	Single gate access		Selective gate driving	
	E_{on} (µJ)	E_{off} (µJ)	E_{on} &(µJ)	E_{off} (µJ)
1	142	3.54	113	5.80
8	195	7.64	89.2	12.4
5	-	-	139	9.67
avg	168.5	5.6	113.7	9.3

B. *Gate-sensitive parameters*

This section presents two unique characteristics not otherwise possible without individual die control: individual junction temperature estimation (using the internal gate resistance) and on-state voltage estimation (using the input capacitance) without any power terminal connection. It is important to state that both methods of acquiring information relevant to the health state of the power module are performed during nominal operation and does not require interruption of the industrial process.

The gate path circuit is commonly modelled as a series RC network for the MOS devices such as IGBTs and MOSFETs. The dependence of the internal gate resistance on the junction temperature is well known [37-41]. Coexistent with the gate resistance temperature dependence, the internal input gate capacitance, C_{ies} or C_{iss}, of the target semiconductor die is dependent on the drain-gate voltage and on the junction temperature above the flat-band voltage V_{FB} of the semiconductor device [42], in the depletion region.

Critically, in order to make the junction temperature measurement linearly dependent on the internal gate resistance alone, the measurement samples of the gate voltage must occur below the flat-band voltage, in the accumulation region. In this region, the gate-emitter capacitance is not dependent on temperature or frequency or collector-emitter voltage or the load current.

When the gate voltage is greater than the flat-band voltage V_{FB} of the MOS-gate semiconductor die, the internal gate capacitance C_{iss} of the target semiconductor die becomes dependent on the drain-gate voltage, as well as the internal junction temperature, described in [42,43].

One technique of measuring the internal gate resistance and the input gate capacitance by using one and the same circuitry is to inject a small reference current, i_{meas}, into the gate terminal of a specific die and then measure the related gate voltage, V_{out}, as shown in Fig. 7 and described in [41].

Fig. 7 shows how multiplexing and control MOSFETs $En_{,n}$ are placed in between the negative power supply rail and the source of a standard totem pole gate buffer, from Fig. 6. In normal operation these control MOSFETs shunt the DC measurement current source, I_{meas}, and make the source potential of the gate driver equal to the negative power supply reference, V_{ss}. To perform the current injection, the target power die is turned-off, and when the respective control MOSFETs, En_j is opened, the measurement current flows into the gate of the target die.

The measured voltage, V_{out}, is an image of the gate voltage, $V_{g,n}$, and evolves as in Fig. 8. The junction temperature can be determined by sampling the voltage across the control electrodes, V_{out} between the time t_1 and t_2 where only the gate resistance is sensitive to the temperature. At t_2, the flat band voltage is reached. The voltage trajectories between t_2 and t_3 are then sensitive to the drain-source voltage and the temperature.

The normal switching pattern is not modified and the typical time to estimate *Tj* is a few microseconds. Note that only a single current source and ADC is necessary to estimate the *Tj* of each parallel die thanks to the multiplexer MOSFET *Enj*, reducing the associated cost: the optimized bill of materials of the associated electronics represents approximately 15% cost increase to popular industrial grade gate drivers available on the market.

C. Junction Temperature Sensing

Junction temperature estimation using thermally sensitive electrical parameters (TSEPs) in power electronics has seen an intensified interest as it is an essential indicator for the state of health of a power module [1]. However, to the best of the authors' knowledge, the TSEPs from literature cannot uniquely identify the individual die junction temperatures, T_{vj}, and the physical meaning of a single measurement for multi-die power modules indicates either an average or a singular/extreme die within the power module [38]. Therefore, a further advantage of having individual gate access to each die is the ability to interact with each die to perform individual junction temperature estimation. A number of TSEPs can be used with the gate circuit of a power device, and the temperature dependency of the internal gate resistance of the semiconductor device is particularly promising due to its customizable nature during die manufacturing [38-41]. Combining this TSEP with the selective gate driving concept then allows for the individual estimation of the junction temperatures of each die, as highlighted in [42].

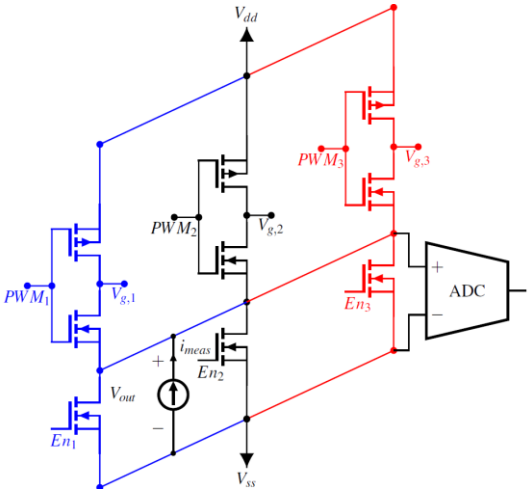


Fig. 7. DC gate injection circuit for a 3 die system with a measurement current *Imeas* and measured gate voltage corresponding to *Vout*

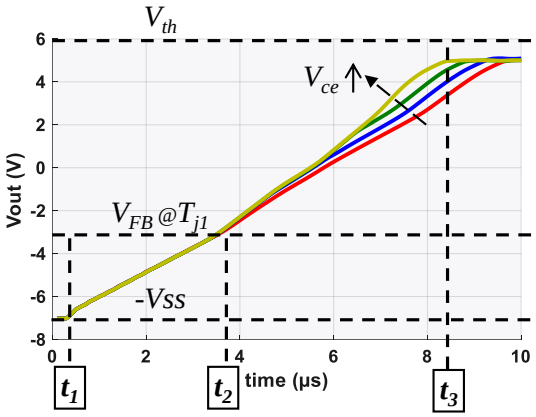


Fig. 8. Experimental waveform of the gate voltage of the inactive die with a constant injection current, and with various blocking voltages, from 0V to 3V, across the inactive die at 25°C (IGBT ref: CM150TX)

As shown in Fig. 9, the simplest way to measure the temperature sensitive gate resistance is to sample V_{out} at time t_1. At this instant, the measured voltage, V_{out}, is proportional to the injected current, i_{meas}, and the internal gate resistance of the die under measurement, $r_{g,n}$, as per (3), but depends on the precision of the current source. In order to cancel the influence of the current source, a pair of samples is taken at instances t'_1 and t''_2. In this period, the gate voltage evolves according to (4). By dividing the second measurement point by the difference between the first and second measurement as per (5), the value of the injected current is no longer present and the equivalent measurement is dependent on timing parameters, as per (6). During the calibration phase, all of the dies are heated at two distinct and known temperatures to determine the linear temperature variation of the gate resistance, i.e. *A* and *B* as per (7). The junction temperature of each die can be estimated

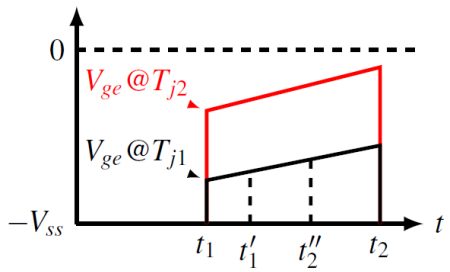


Fig. 9. Injection of the measurement current and corresponding gate voltage with two different values of the internal gate resistance due to two different temperatures, T_{j1} and T_{j2}

during the operation of the power module using the individual current injection on each die according to the selective driving proposed in this paper.

$$V_{out}(t_1) \approx V_{ge}(t_1) = R_g(T_j) \cdot I_{meas} \quad (3)$$

$$V_{ge}(t) = R_g(T_j) I_{meas} + t \cdot \frac{I_{meas}}{C_{ies}} \quad (4)$$

$$TSEP = \frac{V_{ge}(t_1'')}{V_{ge}(t_1'') - V_{ge}(t_1')} \quad (5)$$

$$TSEP = R_g(T_j) \cdot \frac{C_{ies}}{t_1'' - t_1'} + \frac{t_1''}{t_1'' - t_1'} \quad (6)$$

$$T_{j,est} = A \cdot TSEP + B \quad (7)$$

As the measurement occurs below the flat-band voltage of the semiconductor device, the gate-emitter capacitance is not dependent on temperature, and is also invariant to the collector-emitter voltage and load current. This result is confirmed in Fig. 10 (a), where changing the bus voltage, the load current and the switching frequency show no impact on the temperature measurement, where TSEP is obtained as per (5), using the prototype described in Fig. 19.

Further confirming the performance on a six-die IGBT prototype, the Figs. 10 (b) – (c) show two power modules using two different die references with integrated internal gate resistances of 13 Ω and 2 Ω respectively. In the former case, the precision is within 2K with a standard deviation of 0.66K. The latter case has precision of 5K, with a standard deviation of 2.4K. Hence, robust and individual junction temperature measurements are enabled with the selective driving technique.

D. Indirect On-state Voltage Measurements

Another advantage of selective gate driving is that the on-state voltage of the parallel set of dies can be indirectly measured using only the gate circuitry [43]. Consequently, high voltage devices that interface with the power terminals of the power module are not necessary, increasing the reliability of the gate driver.

In the method proposed in this paper, the average on-state voltage of the conducting parallel dies is indirectly measured due to the inactive die blocking the on-state voltage, v_{on} of the parallel dies, as shown in Fig. 11.

Using the same DC measurement current injection circuit as per Fig. 7, the principal operation of the voltage measurement is enabled by increasing the current injection time to change the gate capacitance of the target semiconductor from a voltage-independent state to a voltage-dependent state (Fig. 8). Therefore, one sample between instances t_2 and t_3 must be made to determine the on-state voltage. Consequently, relating V_{out} to v_{on} at a given temperature requires a two-dimensional calibration with linear approximation over small regions of V_{ce}, as per (8).

The indirect saturation voltage measurement by selective gate driving is intended to perform condition monitoring on the interconnections of the power modules, i.e. to detect wire bond lift-off due to aging [1], represented by the resistance $R_{c\,1,2,3}$ and $R_{e\,1,2,3}$ on the Fig. 11. Therefore, the range of voltages to be

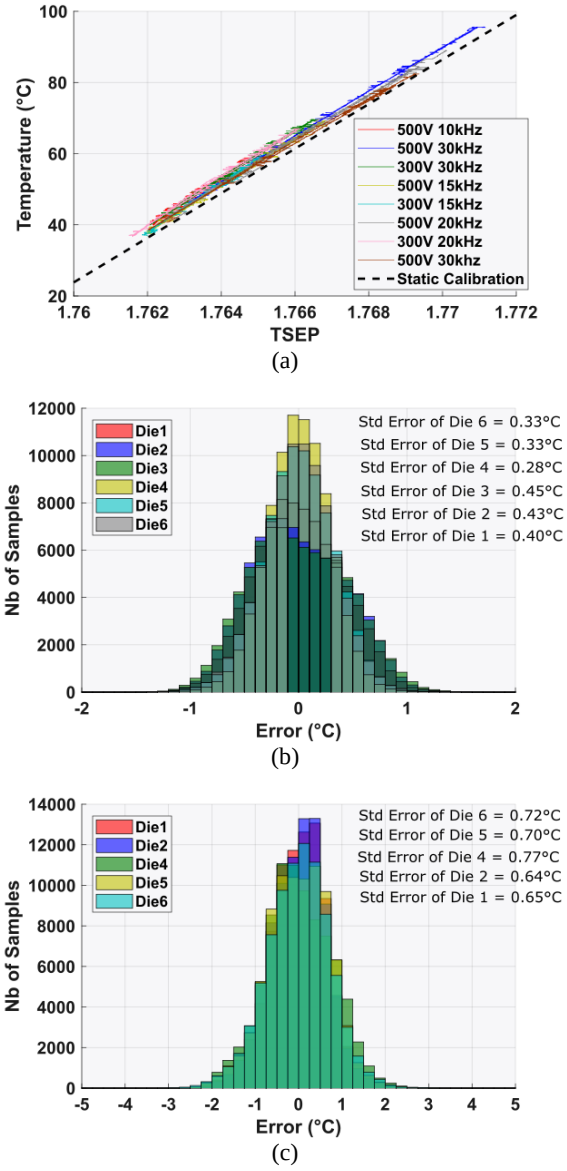


Fig. 10. Experimental junction temperature measurements from prototype of the Fig 19 (a) TSEP as per (5) in function of the temperature variation on the gate of a single IGBT die (Rgint = 13 Ω) under changing dc bus voltage and switching frequency; Temperature dispersion: (b) a power module with 13Ω internal gate resistance; and (c) a power module with 2Ω gate resistance

measured is in the order of 0.5V to 3V, depending on the power semiconductor under test.

Considering this test range, an experimental prototype was passively heated by a hot-plate, and a voltage was applied to the non-conducting device to mimic the reflected voltage of the neighboring dies when in operation.

In (8), each calibration coefficient $C\{T_j\}$ and $D\{T_j\}$ is derived from the calibration at a given junction temperature; more details on the relationship between the measured gate voltage and the corresponding saturation voltage can be found in [43]:

$$v_{on}(T_j) \approx C\{T_j\} V_{out} + D\{T_j\} \quad (8)$$

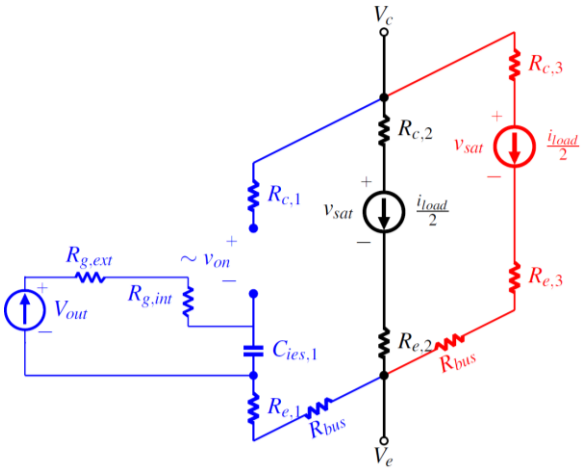
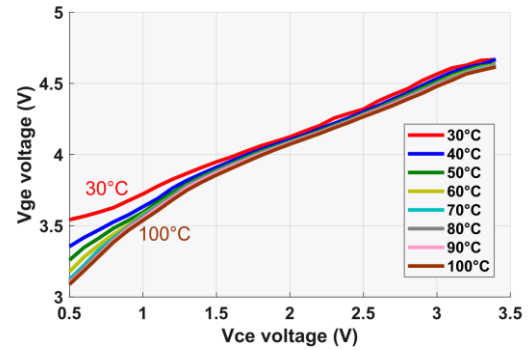


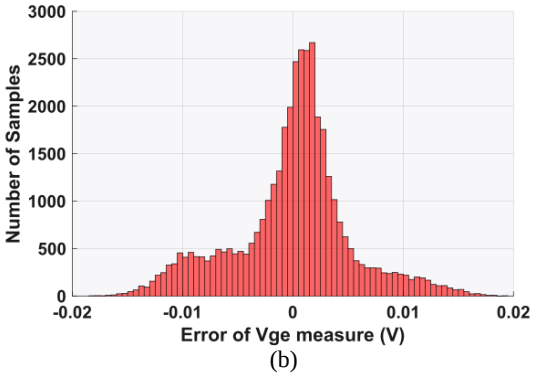
Fig. 11. On-state voltage measurement of the power module: equivalent electric circuit when one device is held off, while the neighboring devices are conducting current

The experimental results, from prototype of Fig. 19, for switching frequency of 20 kHz were plotted in Fig. 12 (a) over the temperature range of 30°C to 100°C. We observe that above V_{CE} of 1.5V, the relationship between V_{CE} and V_{GE} is linear and monotonic and it depends very weakly on the temperature, particularly in the higher temperature range.

Finally, after calibration of the circuit according to (7), Fig. 12 (b) shows that a voltage measurement can be made with a precision of 20mV, and a standard deviation of 6mV.



(a)



(b)

Fig. 12. Experimental on-state voltage measurements from prototype of the Fig 19: (a) increasing blocking voltage of an inactive die with changing gate voltage and temperature; and (b) Distribution of the collector emitter voltage error samples using the described method with selective gate driving and the actual measurement

Assuming slowly-varying load current, the on-state voltage for each die can be obtained by sequentially applying the measurement sequence described above and solving a linear system of equation of order N (number of parallel dies). This enables another important means for condition monitoring of wire-bonded power modules.

IV. Equilibrating the Junction Temperatures

Within parallel-connected pulse-width modulated (PWM) converters, adjusting the individual timing between these converters is used as a means of balancing the switching and conduction losses across the set of converters [25, 44]. Such systems require fast and accurate measurement for the control feedback [45, 46]. Individual timing calibration to match the switching current for paralleled devices is proposed in [26] using an automatic double pulse test bench within a production line. However, the motivation in this paper is to correct the temperature imbalance, as shown in Fig 13, within the power module instead, e.g. due to the thermal constraints caused by the physical location of each die within the power module, and the electrical dispersion of the characteristics of the power dies, especially in the V_{th} of the SiC devices. This is based on the observation that most faults found in practice for power modules are intimately related to temperature. In this sense, the utilization of each die is improved by entirely removing the hot spots from the power module in operation, as it shown in Fig. 13. As the derating in multi-die modules is motivated by the temperature of the hottest die, removing the hot spots by the application of the selective driving pattern effectively allows for an increase in the load current capability of the power module.

The target temperature, $\overrightarrow{Tobj}$, of each die is defined as the average junction temperature, then a loss vector can be found in order to equalize the junction temperature as per (9).

$$\vec{P} = [R_{TH}]^{-1} \times \overrightarrow{Tobj} \tag{9}$$

with $\vec{P} = [P_1, \dots, P_N]^T$ and $\overrightarrow{Tobj} = [\overline{T_J}, \dots, \overline{T_J}]^T$

where $[R_{TH}]$ is the thermal resistance matrix, of size NxN, with the self and coupled thermal resistances and $\vec{P}$ is the sought power dissipation vector of the N dies.

In order to manipulate the power losses and thus the temperature, a delay noted δt_n is applied at the rising edge of the PWM signal, thereby steering the losses in the remaining active dies. The incoming PWM signal is manipulated by the

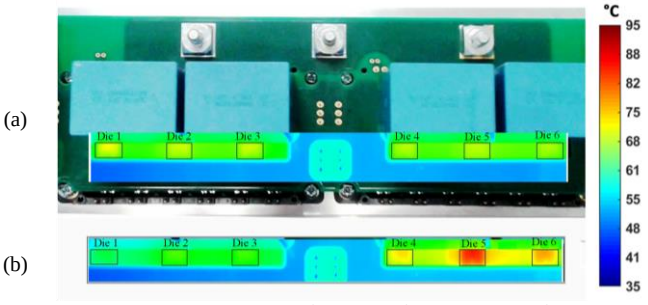


Fig. 13. Temperature distribution of the dies of the prototype of Fig.18 at 78A (a) Thermo-controlled (b) Classical gate driving

CPLD/FPGA controller (Fig 6) and the delay is applied selectively to the hottest dies. Two methods are proposed in this paper.

Firstly, a fixed delay δt can be used to completely eliminate the commutation and (partially) the conduction losses of the selected die during a switching period as it is shown in Fig. 14 (b). The dies that tend to be hotter are delayed more frequently than the colder dies, as detailed in [47]. The delay is determined from a prior knowledge of the temperature distribution of the dies.

In a second solution, a variable delay δt_n is applied to each switching pulse as in Fig. 14 (c). The delay is determined through a closed-loop controller and evolves throughout the life of the power module in response to ageing.

Note that in both cases there is always at least one die commutating with the prescribed instants of the PWM pattern, thus the output PWM waveform on the switching node is not modified in the process.

A. *Fixed Delay Stress Steering*

The control duty cycle, d_j is introduced in eq. (10) and refers to the ratio of the inactivity of the switch j per thermal cycle, Fig. 14 (b). The thermal cycle incorporates a predefined number of sequential switching pulses. Furthermore, the depth of the thermal equalization intervention, d_0, refers to the proportion of normal operation of the power module such that $d_0 = 1 - \sum_{j=1}^{N} d_j$, then the equation (11) is deduced from (10). For example, in Fig. 14, switches 2 and 3 are activated with a delay once within the thermal cycle out of four switching pulses, hence the duty cycle for the first die d_1 is zero and the duty cycles d_2 and d_3 are 25% for dies 2 and 3. The normal operation duty cycle d_0 is therefore 50%. In eq. (13) the loss vector $\overrightarrow{P_0}$ contains the losses of the dies in normal operation and the vectors $\overrightarrow{P_1}$ to $\overrightarrow{P_N}$ contain the losses, $P_{i,j}$, of each die j when the respective die i is activated with the delay δt. Such partial die-shedding pattern is then applied cyclically and relies on the relatively large temperature time constant present in the structure of the power module.

For the purposes of temperature equalization, the duty cycle d_j, is calculated from eq. (12), obtained from eq. (9) and (11). As the duty cycles are limited in the range $0<d_j<1$, an optimization method may be applied to match the temperature requirement with a certain error due to the duty cycle constrains.

$$\vec{P} = \left[\overrightarrow{P_0},\ \overrightarrow{P_1}, \dots, \overrightarrow{P_N}\right] \times [d_0, d_1, \dots, d_N]^T \quad (10)$$

$$\text{with } \vec{P_i} = \left[P_{i,1}, \dots, P_{i,j}, \dots, P_{i,N}\right]^T$$

$$\vec{P} = \left[\overrightarrow{P_1} - \overrightarrow{P_0}, \dots, \overrightarrow{P_N} - \overrightarrow{P_0}\right] \times [d_1, \dots, d_N]^T + \overrightarrow{P_0} \quad (11)$$

$$[d_1 \ \dots \ d_N]^T = \left([R_{TH}] \times \left(\left[\overrightarrow{P_1} - \overrightarrow{P_0}, \dots, \overrightarrow{P_N} - \overrightarrow{P_0}\right]\right)\right)^{-1} \cdot \left(\overrightarrow{Tobj} - [R_{TH}] \times \overrightarrow{P_0}\right) \quad (12)$$

The concept described above was demonstrated using a SiC power converter with forced-air cooling to mimic the operation of the intelligent power module, see Fig. 15. Each power module is composed of 8 parallel discrete devices (ref: C2M0160120D). The power impedance loop has been minimized using decoupling capacitors placed as close as possible of the switching cell to avoid overvoltage during the switching time and the individual gate buffers were similarly placed as close as possible to the power devices. The reference power module has the exact same bus bar layout, but a single gate driver for all the devices, with the gates and sources connected in parallel. The temperature has been measured using only an infrared camera.

The switching losses on the hottest and coldest dies was investigated experimentally on the reference power module and on the multi-gate access power module, as presented in the Table I. Using a fixed delay $\delta t = 20ns$, the switching losses are measured for the switches 5 and 8 while the delay is applied on the switches 4, 5 and 8 on the multi-gate access power module and with the results shown in Table II. The table also shows the ratio of switching energy of the die in tests with delay compared to the measured switching energy without delay but with selective gate driving of Table I.

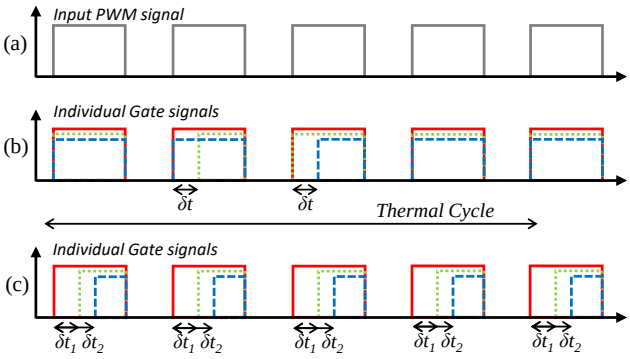


Fig. 14. Selective gate driving (a) switch input PWM signal (b) Individual Gate signals for the Fixed Delay Stress Steering Method (c) Individual Gate signals for the Delay Stress Steering Method

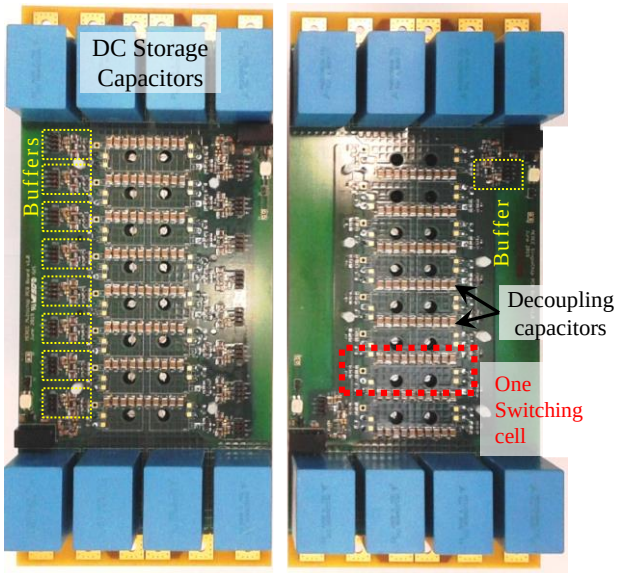


Fig. 15. Experimental prototype composed by 8 paralleled SiC MOSFETs (a) Selective gate driving module (b) Classical driving module

TABLE II
SWITCHING ENERGY OF SELECTIVE GATE DRVING
δt_n = 20ns, VDC = 500V, IDC = 40A, PWM = 200 KHZ

Die Pos.	D4 Delayed by δt_n		D5 Delayed by δt_n		D8 Delayed by δt_n	
	E_{on} (µJ)	Ratio	E_{on} (µJ)	Ratio	E_{on} (µJ)	Ratio
5	171	1.23	19.2	0.13	166	1.19
8	140	1.56	140	1.56	0.64	0.01

In Fig. 16, three temperature distributions on the experimental platform are illustrated: the reference case with a single gate driver for all 8 parallel dies (SG) - the classical way the power modules are driven; the multi-gate driver for the 8 dies with the multi-gate selective driving only ('MG w/o pattern'); and the same module with the application of stress steering with preset delay times ('MG w/pattern). In the reference case, the hottest temperature is 82°C; note that the die at the position 1 is closest to the fan. The threshold voltage dispersion has a significant impact on the thermal distribution across the set of dies. In Fig. 16 (b), the threshold voltages (*Vth*) are plotted with respect to the average *Vth*. High threshold voltage dies exhibit lower losses and lower junction temperature in the case without stress steering for the reference design with classical gate driving. This has been compensated for the module with temperature compensation (traces denoted "MG") and die temperature is equalized despite wide threshold dispersion.

By simply applying the multi-gate access with individual gate buffers, the peak temperature decreases to 68°C (Fig 16a, MG w/o pattern). Note that for the same load conditions the average temperature is reduced, indicating also reduced total losses. This is attributed to more favorable commutation conditions, as indicated in Section III A.

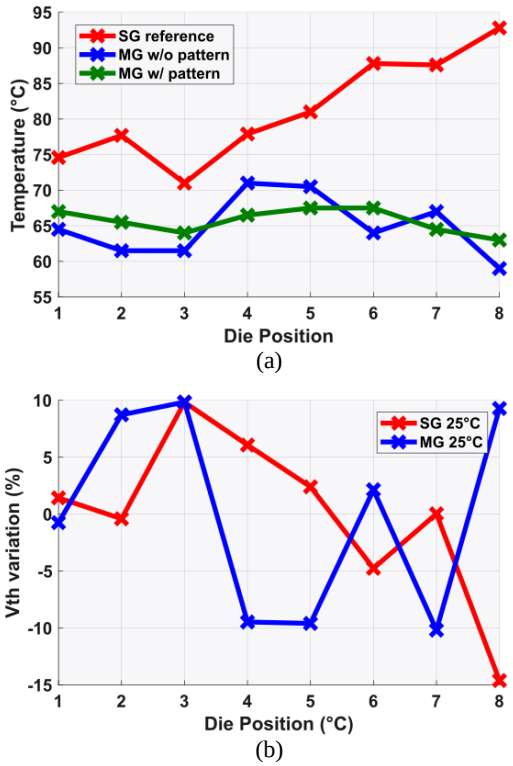


Fig. 16. Experimental data of the classical single gate (SG) and the Multi-gate access (MG) power modules (a) reduction of peak junction temperatures with and without Fixed Delay Stress Steering (w/o pattern) (b) Vth variation on the dies composing the modules

Furthermore, by selectively driving the multi-die controller, using eq. (12) (Fig 16a, MG w/ pattern) with $[d_1, \dots, d_N] = [0.047, 0, 0, 0.243, 0.215, 0, 0.194, 0]$, a further 5°C of peak temperature reduction is gained. This is achieved through re-distribution of the internal power losses by accounting for device parameter and manufacturing spreads based on experimental measurement of the thermal resistance matrix$[R_{TH}]$.

Fig. 17 captures the turn-on transition of 3 out of 8 parallel dies with the thermal equalization pattern applied. The current is commutated within 50ns, after which individual die currents slowly converge to the shared load current value – this is typically seen for parallel dies. We note that Die 5 commutates first, despite the largest delay applied. Similarly, Die8 commutates last despite having applied delay smaller than Die5. It would therefore appear that the applied thermal equalization also contributes to current sharing for the cases where the losses are dominated by switching.

While the method described here is very effective in equating the junction temperatures at a low cost, it necessitates a relatively complex calibration procedure and, more importantly, does not respond to module evolutions such as deteriorating interfaces as ageing progresses

B. Closed-loop, Variable - Delay Stress Steering

This Section describes stress steering that is performed continuously for each die and for each switching pulse. The dies that tend to be hotter are activated with a delay, the duration of which is decided by a closed-loop temperature controller. The delay can be in the range of microseconds for slow-switching devices with predominantly conduction losses or nanoseconds for fast switching devices with predominantly commutation losses.

The target losses of eq. (13) can be described as a function of the unchangeable losses, P_{cte}, such the conduction, turn-off and some amount of the turn-on losses, and the part of the turn-on losses that is modified through the time delay $\overrightarrow{\delta t} = [\delta t_1, \dots, \delta t_n]^T$. These losses, P_{on}, can be approximated by the equation (14), for a delay smaller than the total rising time of

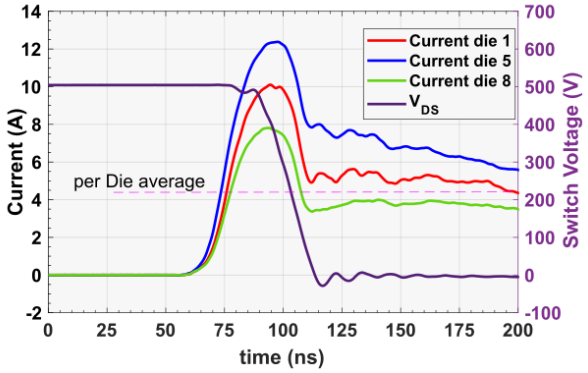


Fig. 17. Experimental waveforms of SiC prototype for a delay of δt = [0, 2.2, 0.8]ns for dies 1, 5 and 8 respectively.

the load current through the switch. The losses modified by the delay P_{on}, correspond to the rising time of the switched current. Then, the commutation time and the total switched current are given in (15) and (16) respectively. Finally, eq. (17) represents the loss distribution between the dies.

$$\vec{P} = \overrightarrow{P_{cte}} + \overrightarrow{P_{ON}}(\vec{\delta t}) \tag{13}$$

$$\overrightarrow{P_{ON}}(\vec{\delta t}) = V_{bus} \cdot F_{PWM} \cdot I_{sw}(\vec{\delta t}) \cdot t_{sw}(\vec{\delta t})/2 \tag{14}$$

$$t_{sw}(\vec{\delta t}) = \frac{I_{Load}}{N \cdot di/dt} + \frac{1}{N} \cdot [M] \times \vec{\delta t} \tag{15}$$

$$I_{sw}(\vec{\delta t}) = \frac{I_{Load}}{N} + \frac{di/dt}{N} \cdot [M] \times \vec{\delta t} \tag{16}$$

$$\text{where : } [M] = \begin{bmatrix} 1-N & 1 & \dots & 1 \\ 1 & 1-N & \ddots & \vdots \\ \vdots & \ddots & \ddots & 1 \\ 1 & \dots & 1 & 1-N \end{bmatrix}$$

with M being a N x N matrix

$$\overrightarrow{P_{ON}} = V_{bus} \cdot F_{PWM} \cdot \left(\frac{di}{dt} \cdot \frac{1}{N^2} \cdot \left([M] \times \vec{\delta t} \right)^2 + \frac{2I_{Load}}{N^2} \cdot [M] \times \vec{\delta t} + \frac{2I_{Load}^2}{N^2 di/dt} \right) \tag{17}$$

The thermal regulation system is shown in Fig. 18 where the applied PWM is modified by the *Temp. Controller* to produce a specific power profile, $\vec{P}$, according to eq. (13). The delay applied to the input PWM pattern for each die can be derived from the error between the average measured temperatures of all the dies, and the individual die temperature using the TSEP-based method. Using this error, a scheduling controller removes or adds delay to each die. The controller is a multivariable proportional integral compensator with the transfer function as per (18) and (19). Hence, the temperature can be balanced between all parallel dies on-line during the operation of the converter.

$$\vec{\delta t} = \vec{\delta t'} - \min(\vec{\delta t'}) \tag{18}$$

$$\vec{\delta t'} = \begin{pmatrix} P + I \cdot s & 0 & \cdots & 0 \\ 0 & \ddots & \ddots & \vdots \\ \vdots & \ddots & \ddots & 0 \\ 0 & \cdots & 0 & P + I \cdot s \end{pmatrix} \cdot (T_j - \bar{T}_j), \tag{19}$$

where s is the Laplace variable

As a demonstration, an air-cooled prototype power module was constructed from two parallel six-pack power modules, CM150TX-24S1 from Mitsubishi Electric, as shown in Fig. 19a. Each switch thus comprises 6 dies, distributed in two different packages. The FPGA employed for prototype is a Xilinx Spartan-6 with a 100 MHz clock, paired with a 16-bit AD7626 ADC). This is incorporated in a back-to-back full bridge converter developed for a 500V dc bus (Fig. 19b). The temperature has been measured using the TSEP-based method described in section III-C and verified with an infrared camera.

Loading the prototype power module causes an unequal temperature distribution across the set of parallel dies, with a maximum difference of 23°C from the coldest to hottest die, as shown in Fig. 20 (a) (Open Loop). This dispersion is attributed to the air cooling employed, inequality in thermal paths and die parameter dispersal. The maximum current handling capability of the power module is limited by the hottest die, in this case Die5. After enabling the temperature balancing control, the maximum temperature at the same loading condition decreases towards the mean temperature by 12°C, and the previously coldest die increases by nearly the same amount, as shown in Fig. 20 (a) (Closed Loop). In this case, if the load current capability is fixed by the maximum junction temperature of any given die, the power module with more even thermal loading is capable of withstanding more losses. Therefore, the load

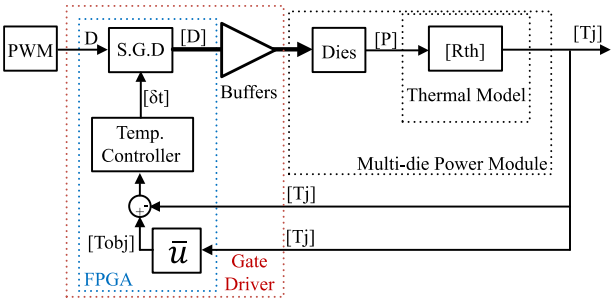


Fig. 18. Selective gate driving: reduction of peak junction temperatures with application of a driving profile for a power module with multi-gate (MG) access compared to the reference single gate (SG) power module

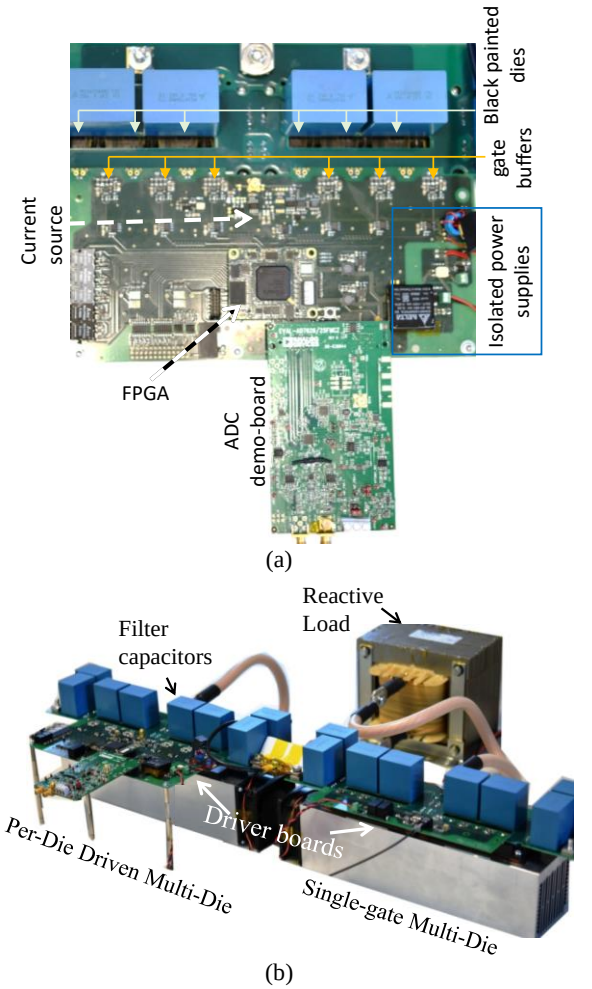


Fig. 19. Experimental IGBT prototype (a) gate driver with junction temperature measurement as per Fig 6 and 7 (b) back to back configuration

current can be increased, and the power density of the power module can be improved. Importantly, the above experiment also demonstrates the method applied to a set of dies distributed in two separate packages, addressing also the problem of stress sharing between parallel power modules. Also, the closed-loop method will sustain this stress distribution throughout the lifecycle of the module.

In order to better visualize the effect of balancing the die temperatures on the load current handling capability of the power module, Fig. 20 (b) illustrates the power module with no selective driving pattern applied (i.e. open loop with no temperature balancing) and closed loop conditions (i.e. with temperature balancing for a given load current). As an example, on the 25A point, the controller applies a delay equals to $\overrightarrow{\delta t} = [0,\ 140, 70, 140, 300, 160]ns$ on the dies 1 to 6 respectively. As the load current increases, the difference between the maximum junction temperatures of the two solutions increases. Hence, for a fixed maximum junction temperature, there is an associated load current handling capability of the power module. In this experimental prototype, the selective gate drive method permits an increase of 25% in the current handling capability, assuming a maximum junction temperature of 150°C for the hottest die.

Table III shows the maximum and average temperatures for the operating points of Fig. 20. While the maximum temperature could be reduced for all operating points, the average temperature is maintained in a range of +/-1°C, the precision of the temperature measurement. This indicates that the efficiency of the multi die power module is unaffected by the applied stress-steering.

A demonstration video of the on-line thermal equalization is shown in [49]. The switch to thermal equalization mode, performed in real time, occurs at 1min31s in the video.

TABLE III
JUNCTION TEMPERATURES
VDC = 500V, PWM = 10 KHZ, TAMB = 25°C

Current (A)	Junction temperatures (°C)					
	Maximum			Average		
	O.L.	C.L.	Diff.	O.L.	C.L.	Diff.
10	34,2	34,1	-0,1	31,8	32,0	0,2
25	45,5	43,4	-2,0	41,0	41,2	0,2
30	50,2	46,4	-3,8	44,9	44,4	-0,5
45	60,3	54,8	-5,5	53,1	53,0	-0,1
65	74,6	66,4	-8,2	64,7	65,4	0,7
78	85,6	74,8	-10,7	73,5	73,9	0,4

V. Conclusion

In this paper, a method that implements selective gate driving for an intelligent power module is presented as a solution to accommodate the use of smaller, more numerous dies within a multi-die power module. By incorporating individual gate driving, the switching losses can be reduced, and several condition monitoring features such individual junction temperature estimation and indirectly measuring the saturation voltage in the power module can be performed. Furthermore, by incorporating the individual junction temperature estimation and the selective gate driving technique, the individual dies within the power module can be better utilized, thereby

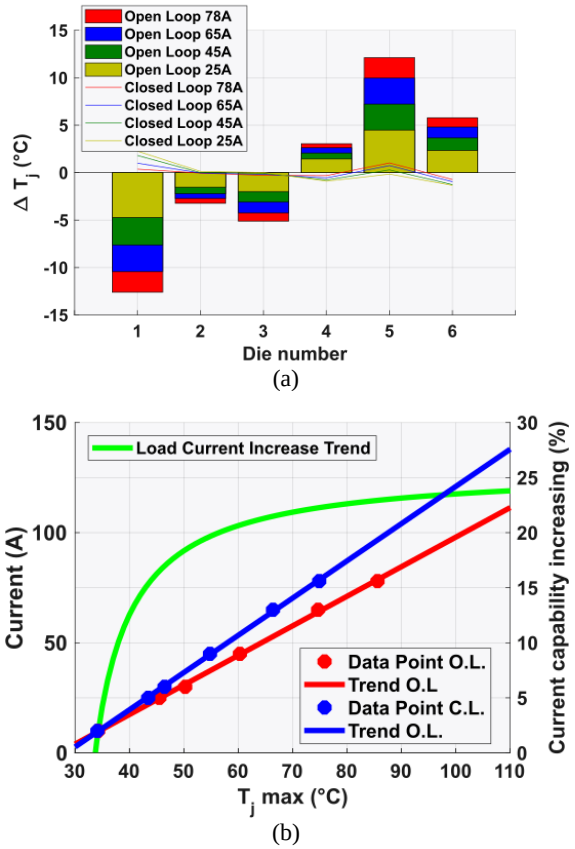


Fig. 20. Application of temperature balancing the prototype power module at 500V and 10 kHz (a) difference in temperature relative to the mean temperature with balanced and unbalanced temperatures and (b) load current handling capability increase

enabling a substantial increase in the load current handling capability of the power module. The technique presented in this paper is applicable to highly integrated large-current intelligent power modules based on wide bandgap semiconductors with inherently smaller, more numerous dies.

An interesting corollary to the proposed thermal equalization solution is that it enables unrestricted paralleling of small power modules to achieve a very large current rating which, together with the inherent condition monitoring features, would allow significant cost reductions for high power, mission-critical applications.

Finally, a switching power cycling tests bench has been running the proposed junction temperature algorithm consistently for over 2 years. The resulting lifetime extension and the use of the generated data for condition monitoring purposes will be discussed in a forthcoming paper.

References

[1] H. Wang, M. Liserre, and F. Blaabjerg, "Toward reliable power electronics: Challenges, design tools, and opportunities," *IEEE Ind. Electron. Mag*., vol. 7, no. 2, pp. 17–26, 2013.

[2] 'The Highly Efficient and Reliable smart Transformer (HEART)' [online], http://www.heart.tf.uni-kiel.de/en/home/

[3] 'Reliable Power Electronics (ReliPE)' [online], https://www.sintef.no/en/reliable-power-electronics/

[4] E. A. Jones, F. F. Wang, and D. Costinett, "Review of Commercial GaN Power Devices and GaN-Based Converter Design Challenges," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 4, no. 3, pp. 707–719, 2016.

[5] J. Roberts, J. Styles, and D. Chen, “Integrated gate drivers for e-mode very high power GaN transistors,” *IEEE Int. Work. Integr. Power Packag. IWIPP 2015*, pp. 16–19, 2015.

[6] M. Giandalia and D. Kinzer, “System integration benefits of GaN Power ICs,” in PCIM Europe 2019 - *International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, Nuremberg, 2019.

[7] H. Li et al., "Influence of Paralleling Dies and Paralleling Half-Bridges on Transient Current Distribution in Multichip Power Modules," *IEEE Transactions on Power Electronics*, vol. 33, no. 8, pp. 6483-6487, Aug. 2018.

[8] S. Weihua, L. Ran, Z. Zheng, L. Xiaoling and P. Mawby, "Design and evaluation of SiC multichip power module with low and symmetrical inductance," *The Journal of Engineering*, vol. 2019, no. 17, pp. 3573-3577, 6 2019.

[9] C. Chen, F. Luo and Y. Kang, "A review of SiC power module packaging: Layout, material system and integration," *CPSS Transactions on Power Electronics and Applications*, vol. 2, no. 3, pp. 170-186, Sept. 2017.

[10] J. Ewanchuk, J. Brandelero, and S. V. Mollov, “Improving the Die Utilization and Lifetime in Multi-die SiC Power Module by Means of Integrated Per-die Gate Buffers,” *Proceedings of the 29th International Symposium on Power Semiconductors and Devices & ICs*, 2017.

[11] J. Ewanchuk, J. Brandelero and S. Mollov, "A Gate Driver Based Approach to Improving the Current Density in a Power Module by Equalizing the Individual Die Temperatures," *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, Portland, OR, 2018, pp. 4652-4658.

[12] S. Zhao et al., “Adaptive Multi-Level Active Gate Drivers for SiC Power Devices,” *IEEE Trans. Power Electron.*, vol. PP, no. c, pp. 1–1, 2019.

[13] Y. Yang, Y. Wen, and Y. Gao, “A Novel Active Gate Driver for Improving Switching Performance of High-Power SiC MOSFET Modules,” *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 7775–7787, 2018.

[14] A. P. Camacho, V. Sala, H. Ghorbani, and J. L. R. Martinez, “A Novel Active Gate Driver for Improving SiC MOSFET Switching Trajectory,” *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 9032–9042, 2017.

[15] G. Engelmann, T. Senoner, and R. W. De Doncker, “Experimental Investigation on the Transient Switching Behavior of SiC MOSFETs Using a Stage-Wise Gate Driver,” *CPSS Trans. Power Electron. Appl.*, vol. 3, no. 1, pp. 77–87, 2018.

[16] Y. Avenas, L. Dupont, N. Baker, H. Zara, and F. Barruel, “Condition Monitoring: A Decade of Proposed Techniques,” *IEEE Ind. Electron. Mag.*, vol. 9, no. 4, pp. 22–36, 2015.

[17] U.-M. Choi, F. Blaabjerg, S. Jorgensen, S. Munk-Nielsen, and B. Rannestad, “Reliability Improvement of Power Converters by Means of Condition Monitoring of IGBT Modules,” *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7990–7997, 2017.

[18] H. Oh, B. Han, P. Mccluskey, C. Han, and B. D. Youn, “Physics-of-Failure, Condition Monitoring, and Prognostics of Insulated Gate Bipolar Transistor Modules: A Review,” *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2413–2426, 2015.

[19] M. A. Eleffendi and C. M. Johnson, “Application of Kalman Filter to Estimate Junction Temperature in IGBT Power Modules,” *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1576–1587, 2016.

[20] B. Ji et al., “In situ diagnostics and prognostics of solder fatigue in IGBT modules for electric vehicle drives,” *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1535–1543, 2015.

[21] T. A. Polom, C. van der Broeck, R. W. De Doncker, and R. D. Lorenz, “Real-Time , In Situ Degradation Monitoring in Power Semiconductor Converters,” *2019 IEEE Appl. Power Electron*. Conf. Expo., pp. 2720–2727, 2019.

[22] X. Wang, et al., "Current sharing of IGBT modules in parallel with thermal imbalance," *2010 IEEE ECCE*, Atlanta, USA

[23] N. Chen, F. Chimento, M. Nawaz, and L. Wang, “Dynamic Characterization of Parallel-Connected High-Power IGBT Modules,” *IEEE Trans. Power Electron.*, vol. 51, no. 1, pp. 539–546, 2015.

[24] H. Li et al., “Influences of device and circuit mismatches on paralleling silicon carbide MOSFETs,” *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 621–634, 2016.

[25] P. Hofer, N. Karrer, and C. Gerster, “Paralleling intelligent IGBT power modules with active gate-controlled current balancing,” *PESC Rec. 27th Annu. IEEE Power Electron. Spec. Conf.*, vol. 2, pp. 1312–1316, 1996.

[26] S. Teuber, M. Honsberg, A. Kubitz and G. Katzenberger, "IGBT Power Stage Delay Calibration is Minimizing Current Imbalance in Large Power modules with isolated multiply segmented paralleled half bridges," *PCIM Europe 2018; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, Nuremberg, Germany, 2018, pp. 1-7.

[27] K. Matsubara and K. Wada, "Current Balancing for Parallel Connection of Silicon Carbide MOSFETs Using Bus Bar Integrated Magnetic Material," *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Anaheim, CA, USA, 2019, pp. 2688-2693.

[28] J. Wang, Z. Li, X. Jiang, C. Zeng and Z. J. Shen, "Gate Control Optimization of Si/SiC Hybrid Switch for Junction Temperature Balance and Power Loss Reduction," *IEEE Transactions on Power Electronics*, vol. 34, no. 2, pp. 1744-1754, Feb. 2019.

[29] Z. Zeng, X. Zhang and X. Li, "Layout-Dominated Dynamic Current Imbalance in Multichip Power Module: Mechanism Modeling and Comparative Evaluation," *IEEE Transactions on Power Electronics*, vol. 34, no. 11, pp. 11199-11214, Nov. 2019.

[30] B. Zhang and S. Wang, "Parasitic Inductance Modeling and Reduction for a Wire Bonded Half Bridge SiC MOSFET Multichip Power Module," *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Anaheim, CA, USA, 2019, pp. 656-663.

[31] S. Weihua, L. Ran, Z. Zheng, L. Xiaoling and P. Mawby, "Design and evaluation of SiC multichip power module with low and symmetrical inductance," *The Journal of Engineering*, vol. 2019, no. 17, pp. 3573-3577, 6 2019.

[32] H. Li, et al., "A Novel DBC Layout for Current Imbalance Mitigation in SiC MOSFET Multichip Power Modules," *IEEE Trans. Power Elect.*, vol. 31, no. 12, pp. 8042-8045, Dec. 2016.

[33] D. Reusch and J. Strydom, "Effectively paralleling gallium nitride transistors for high current and high frequency applications," *2015 IEEE Applied Power Electronics Conference and Exposition (APEC), Charlotte*, NC, 2015, pp. 745-751.

[34] Z. Zeng, X. Zhang, and X. Li, “Influence of Kelvin Connection on Current Dispatching in Multichip Power Module: Mechanism Modeling and Comparative Evaluation,” *IEEE Trans. Power Electron.*, vol. PP, no. c, pp. 1–1, 2019.

[35] Y. Xiao, H. Shah, T. P. Chow, and R. J. Gutmann, “Analytical modeling and experimental evaluation of interconnect parasitic inductance on MOSFET switching characteristics,” *IEEE Appl. Power Electron. Conf. Expo. 2004. APEC ’04.*, vol. 1, no. C, pp. 516–521, 2004.

[36] N. Chen, F. Chimento, M. Nawaz, and L. Wang, “Dynamic Characterization of Parallel-Connected High-Power IGBT Modules,” *IEEE Trans. Ind. Appl.*, vol. 51, no. 1, pp. 539–546, 2015.

[37] M. Denk and M. Bakran, “Comparison of U CE - and R Gi -based Junction Temperature Measurement of Multichip IGBT Power Modules Keywords 1 Introduction 2 Measurement methods and test setup,” *2015 17th Eur. Conf. Power Electron. Appl. (EPE’15 ECCE-Europe)*, pp. 1–11, 2015.

[38] N. Baker, L. Dupont, S. Munk-Nielsen, F. Iannuzzo, and M. Liserre, “IR camera validation of IGBT junction temperature measurement via peak gate current,” *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 3099–3111, 2017.

[39] N. Baker, S. Munk-Nielsen, F. Iannuzzo, and M. Liserre, “IGBT Junction Temperature Measurement via Peak Gate Current,” *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3784–3793, 2016.

[40] M. Denk and M. Bakran, “Junction Temperature Measurement during Inverter Operation using a T J -IGBT-Driver,” *PCIM Europe*, 2015, Nuremberg, Germany.

[41] J. Brandelero, J. Ewanchuk and S. Mollov, "On-line Virtual Junction Temperature Measurement via DC Gate Current Injection," *CIPS 2018; 10th International Conference on Integrated Power Electronics Systems*, Stuttgart, Germany, 2018, pp. 1-7.

[42] N. Baker and F. Iannuzzo, “The Temperature Dependence of the Flatband Voltage in High-Power IGBTs,” *IEEE Trans. Ind. Electron.*, vol. 66, no. 7, pp. 5581–5584, 2019.

[43] J. Brandelero, L.M. Alonso, J. Ewanchuk, and S. V. Mollov, “Indirect On-State Voltage Estimation Using a Voltage Sensitive Electrical

Parameter through the Gate Driver" *PCIM Europe 2019*, Nuremberg, Germany.
[44] D. Bortis, P. Steiner, J. Biela, and J. W. Kolar, "Double-stage Gate Drive Circuit for Parallel Connected IGBT Modules," *IEEE Trans. Dielectr. Electr. Insul.*, vol. 16, no. 4, pp. 1020–1027, 2009.
[45] Y. Lobsiger, D. Bortis and J. W. Kolar, "Decentralized active gate control for current balancing of parallel connected IGBT modules," *Proceedings of the 2011 14th European Conference on Power Electronics and Applications, Birmingham*, 2011, pp. 1-10.
[46] Ying Chen, Fang Zhuo, Wenjie Pan, Fan Zhang, Lei Feng, "A novel active gate driver for static and dynamic current balancing of parallel-connected IGBTs", *2017 IEEE Applied Power Electronics*
[47] J. Ewanchuk, J. Brandelero and S. Mollov, "Lifetime extension of a multi-die SiC power module using selective gate driving with temperature feedforward compensation," *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Cincinnati, OH, 2017, pp. 2520-2526.
[48] J. Lu, R. Hou and D. Chen, "Loss Distribution among Paralleled GaN HEMTs," *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, Portland, OR, 2018, pp. 1914-1919.
[49] 'Thermal equalization Video [online], https://youtu.be/hPBHLPJ7KXU

J. Brandelero (M'16) received his B.S from the Federal University of Santa Catarina, Brazil, and his B.S and M.S from the INPT – ENSEEIHT in Toulouse-France. He received his Ph.D. degree from the National Polytechnic Institute of Toulouse in 2015 with the Laplace Laboratory and Cirtem. His research activity focused on power electronics application in the field of the more electrical aircraft. In 2015, he joined the Power Electronic Systems Division at the Mitsubishi Electric R&D Centre Europe in Rennes where he conducts research related to condition monitoring, reliability and robustness of power converters.

J. Ewanchuk (M'13) received the B.Sc. degree (with distinction) in electrical engineering, M.Sc. degree with a specialization in power electronics, and a PhD degree in Energy Systems from the University of Alberta, Canada, in 2006, 2008 and 2012, respectively.
From 2008 to 2009, he was a Design Engineer with RMS Welding Systems, Nisku, Canada. In 2012, he joined Mitsubishi Electric Research Centre Europe in Rennes, France as a Research Engineer in power electronics, afterwards taking position as a Senior Staff Research Engineer, and then later as a Research Manager. Since 2019, he has been a Staff Engineer in Power Electronics Packaging with the Research Center at Raytheon Technologies, in East Hartford, USA. His current research interests include highly integrated power converters, high density packaging concepts, and the design consequences on the power converter lifetime and robustness.

S. Mollov (M'87) received the Dipl. Eng. degree from the Technical University of Gabrovo, Bulgaria, in 1995, and the Ph.D. degree from the University of Birmingham, U.K. From 2000, he was a Lecturer with the University of Birmingham, where his research activities focused on power electronics applications in the field of autonomous systems, aerospace electrical systems, and renewable energy sources and storage. In 2005, he joined ADETEL Group, France, as a Power Electronics Expert, working on transportation applications. In 2009, he joined THALES Avionics as a Power Supply Expert. Since 2013, he has been the Head of the Power Electronic Systems Division at the Mitsubishi Electric R&D Centre Europe, Rennes, France, with activities covering reliability, diagnostics & prognostics and optimal design of highly integrated power conversion equipment.