MITSUBISHI ELECTRIC R&D CENTRE EUROPE

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Internship proposal (6 months)

Ref DITIN023

Design of a Gate Driving Circuit with Dead-time optimizer and low-Jitter feature

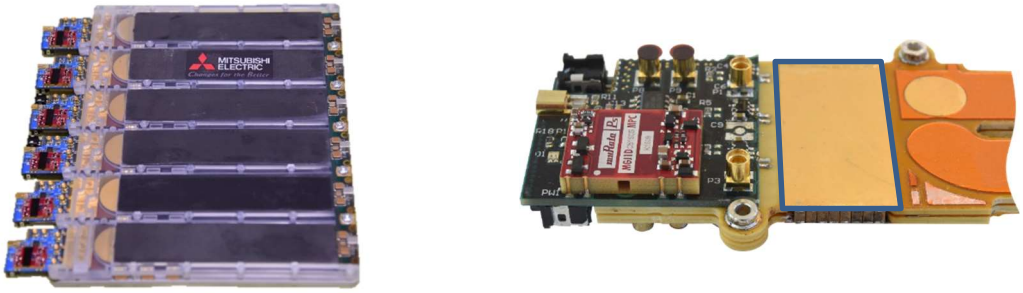
Internship supervisors

Mitsubishi Electric R&D Centre Europe**:** Johan Le Leslé, Researcher
IETR Nantes: Nicolas GINOT, Professor

Overall context

Mitsubishi Electric R&D Centre Europe (MERCE) is the European R&D center from the Corporate R&D organization of Mitsubishi Electric. The aim of our center is to provide advanced R&D support to the Japanese R&D centers and to the business units of Mitsubishi Electric Corporation. Situated at the heart of Europe's leading R&D community, MERCE conducts R&D into next generation communication systems, and technologies related to Energy and Environment. Design of next generation power converter is a major activity in the Power Electronic System division (PES)

The PES division is divided into two teams: the **D**esign & **I**ntegration **T**echnology (DIT) and the **H**ealth **M**anagement **T**echnology (HMT). DIT team is actively working on advanced packaging for Power Electronics and high density/high efficiency power converters for E-mobility – see Fig 1.



a) b)

Fig.1 Example of highly integrated DC/DC converter for automotive purpose[1].a) Overall converter with six interleaved power building block. b) Zoom on the power building block highlighting the area of PCB embedded dies (blue rectangle) and associated gate driver.

Internship subject

Over the past years, MERCE has developed several technological solutions for driving units, intending to speed up the switching transitions safely or protecting devices from short-circuit. To get the best out of the latest generation of Wide Band Gap semiconductor devices, it is also mandatory to implement reduced deadtimes, mostly for loss reduction in systems operating at high switching speed (hundreds of kHz to MHz).

[1] Press release March 25, 2020 : https://www.mitsubishielectric.com/news/2020/0325.html

However, the system can lead to dramatic failures if the deadtimes are too short, both switches being conductive simultaneously. Such issues may also occur in case of timing mismatch (jitter), even with properly selected deadtime during the original design process.

Therefore, your objective, as a member of the DIT team, is to lead the design of a functional driving unit with minimized deadtimes while being immune to jitter. The cornerstone of this solution is an electronic topology patented by MERCE in 2022, but not experimented yet.

At first, you will get familiar with the foreseen concept through circuit simulations, this concept is still open to improvements based on your vision and propositions for the technological choices. Then, an important part will be the experimental validation, of the different functional blocks at the begin, and of the overall system at the end. This system is composed of the high-performance gate driver, and of an optimized switching cell made of SiC or GaN devices, which you will also be in charge of the design.

Therefore, if you have the will to work for an international company developing cutting-edge technologies, if you are passionate about electronics, power electronics, experiments, do not hesitate and join us.

Detailed objectives / organization

The internship is in collaboration with the IETR Nantes and will take place at the IETR facilities and in MERCE premise, and will entail the following tasks:

- Design of the functional driver (Pre-driver + Push-Pull)
- Validation of the negative gate current detector used for synchronizing semiconductor devices
- Technological identification for the insulation technology (Bandwidth, propagation delays)
- Design of the conditioning part (Deadtime minimizer)
- Debug of the overall circuitry on a real platform
- If possible, quantification of the gain with respect to losses (w. vs. wo. Deadtime optimizer)

Prerequisites

- Engineer/Master level student with interest in research.
- Understanding of power electronics mechanisms.
- Strong interest in experimentation, and familiar with basic electrical engineering lab equipment.
- Autonomous, but team player.
- English: spoken / written.

Duration: 6 months

Period: from Feb/March 2023 (possibility of flexibility, depending on schools' internships periods)

Contact : Magali BRANCHEREAU (jobs@fr.merce.mee.com) + Johan Le Leslé

Thank you to provide us an application letter and your CV mentioning the reference of the internship.

The signature of an Internship Agreement with your school is mandatory.