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PhD Thesis proposal (3 years)

Reference DITFT038

Design of a smart-low consumption gate driver for high-frequency operations of parallel PCB embedded dies

PhD Thesis supervisors:

Mitsubishi Electric R&D Centre Europe**:** Johan Le Leslé, Researcher
IETR Nantes: Nicolas Ginot, Anne-Sophie Descamps, Christophe Batard

Overall context

Mitsubishi Electric R&D Centre Europe (MERCE) is the European R&D center from the Corporate R&D organization of Mitsubishi Electric. The aim of our center is to provide advanced R&D support to the Japanese R&D centers and to the business units of Mitsubishi Electric Corporation. Situated at the heart of Europe's leading R&D community, MERCE conducts R&D into next generation communication systems and technologies related to Energy and Environment. Design of next generation power converter is a major activity in the Power Electronic System division (PES)

Thesis subject

The PES division is divided into two groups: the **D**esign & **I**ntegration **T**echnology (DIT) and the **H**ealth **M**anagement **T**echnology (HMT). DIT group is actively working on advanced packaging for Power Electronics and high density/high efficiency power converters– see Fig 1.

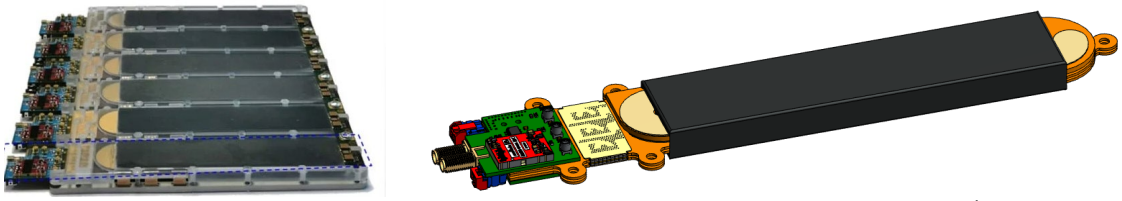

Fig.1 Example of highly integrated DC/DC converter for automotive purpose[1]

Over the past years, MERCE has been developing several technological solutions for driving units, with the motivation being to get the best out of the latest generation of Wide Band Gap devices and further increase the switching frequency, up to the MHz range. Therefore, several patented concepts were applied to speed up the switching transition, reduce the dead-time safely or protect devices from short-circuit. In such medium to high power system using several dies in parallels, the gate driving unit is a key stone. Two main challenges can be highlighted:

1. Reduction of the gate driver consumption: increase the switching frequency in conjunction with a high number of dies to be simultaneously driven is indeed putting a strain on the gate driver as the required gate drive power is as follow: $P_{GD} = \Delta V_G \cdot Nb_{Dies} \cdot Q_G \cdot fsw$. So, the gate driver power supply rating will increase, so as the size, which is opposing with the high-power density and high efficiency philosophy. To overcome this bottleneck, some gate drive architecture allows to partially recover the gate charge, being a key feature to

[1] Press release March 25, 2020 : https://www.mitsubishielectric.com/news/2020/0325.html

maintain a low footprint and reduce the gate driver contribution into the overall system losses. [1], [2]

2. The second challenge deals more specifically with the parallelisation of dies. It turns out that by having several unitary devices, with their own characteristics (V_{Th}, gm, R_G, etc), sharing the same package, but not necessarily having the same fanout for the power and the gate interconnections can lead to unbalanced current distribution, in particular during the switching events. Those deviations can be mitigated with smart gate drivers with unitary gate control, as already done in some research works for IGBT and Si/SiC MOSFETs [3]–[5]. However, the conventionally employed packaging or PCB layouts, were one of the main contributors to these unbalances mainly because of high and unbalanced stray inductances. By moving to high performance packaging, such as PCB embedding, stray inductances are drastically lowered, the switching transients become much faster, so the conventional current balancing method might not be properly effective.

The main objective of the proposed thesis subject is to propose a gate drive architecture being compact and addressing the two aforementioned issues.

Detailed objectives / organization

The thesis will take place in MERCE and IETR premises and will entail the following tasks:

- Study the state-of-art for low consumption gate driver and current balancing control methods
- Design, optimisation and evaluation of a gate driver enabling the gate charge recovery
- Design, optimisation and evaluation of a gate drive for current unbalance control
- Conception of a final prototype integrating both features
- Redaction of quarterly reports
- Redaction and publication of scientific papers
- Redaction of the thesis manuscript
- PhD defence

Prerequisites

- Engineer/Master degree with interest in research;
- Understanding of power electronics mechanisms.
- Having competences in LtSpice simulations applied to power electronic switching cell associated to its gate driver
- Having competence in Matlab for circuit design optimisation and/or experimental data analysis
- Strong interest in experimentation, and familiar with basic electrical engineering lab equipment. (Power supplies, scope, Pulse generator, etc)
- Having a first experience on designing an analogue based smart driver for dead-time reduction for WBG device would be a must
- Autonomous, but team player.
- English: spoken / written.

Duration: 3 Years

Period: from July 2025 to July 2028

Contact: Magali BRANCHEREAU (jobs@fr.merce.mee.com) + Johan Le Leslé

Thanks for providing us an application letter and your CV mentioning the reference of the PhD thesis

References

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